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A recent federally funded study estimated that corrosion costs the US economy $276B/year, with the DoD’s share being in excess of $20B/year. A major factor responsible, in-part, for creating these costs is that designers tasked with performing materials selection are typically not trained to carry out rigorous corrosion analyses. Increasing corrosion knowledge through enhanced engineering curricula at our nation’s colleges and universities will, over the long-term, help reduce the severity of the problem. However, the DoD’s Reliability Information Analysis Center (RIAC) believes that complementing the improved educational practices by initiating a comprehensive, interdisciplinary program that mobilizes engineering specialties not currently involved in fighting corrosion will create a new paradigm that will help accelerate the solution to this critical problem.

The best way to universally reduce the cost of corrosion would be for the materials engineering community to actively support both the design and sustainment phases of the system life cycle. For years, this community has tried to play a greater role, but some perceptions concerning the value of support that materials engineers could provide has caused designers, logisticians and program managers to view their involvement as an unaffordable luxury. This barrier is unlikely to ever be overcome except for situations where either serious problems arise or when a design’s operational requirements demand exceptional materials performance.

Fully benefiting from the capabilities and technologies developed by the materials community will take a new approach. The RIAC believes that a program to re-engineer existing corrosion prevention and control (CP&C) practices and technologies and integrate them into the processes currently employed by an engineering discipline that has a well-defined role in the systems engineering process is the best way to ultimately solve the corrosion problem. Our approach, as described in this article, is specifically designed to complement ongoing educational initiatives by providing a near-term mechanism for increasing effective consideration of CP&C. This approach also provides for sustainable long-term implementation since it incorporates provisions to institutionalize the proposed measures by having them integrated into a formal professional certification program.

Reliability Engineering - The Logical Candidate

Broadly implementing a process to overcome current limitations with respect to fully considering corrosion during product design and sustainment can only be accomplished if the ‘stovepipes’ responsible for impeding the utilization of existing technology and practices are overcome. Corrosion knowledge and skills are currently compartmentalized within the materials engineering community, a discipline that often finds itself on the outside looking in with respect to product design and sustainment efforts. This community has long tried to increase its involvement in the design and sustainment phases of the system lifecycle, and, in certain instances, it has been successful. A prime example is the aerospace industry, where materials engineers routinely support design actions to ensure that system components and structures are both lightweight and durable. However, for the vast majority of product development efforts, materials are viewed as commodity products that don’t require any specific expertise to employ. Since program managers typically see little benefit to using precious development funding to engage materials professionals, the technologies developed by the community, including those related to corrosion, are often overlooked.

Effectively overcoming the stovepipes that limit the employment of corrosion technologies requires a re-examination of current engineering practice. Since it’s doubtful that materials engineers will ever routinely become fully engaged in system design and sustainment, then an alternate approach is to find a new ‘standard bearer’; a technical community with an existing charter and well-recognized role that will facilitate including CP&C considerations into the system engineering process; a technical community willing to expand its traditional methodologies by also considering CP&C as it relates to design and sustainment and, thus, help solve this pervasive problem.

The reliability engineering community is the logical candidate for taking on an expanded role, since the discipline is already an essential component of the systems engineering process and, also, because corrosion is a significant reliability limiting failure mechanism in systems and products. As a
horizontally integrated engineering function, reliability engineers currently work with and support many engineering disciplines, including specialties supporting the research, development, acquisition, operation and sustainment spectrums of the system life cycle. As a result, the insight this community possesses concerning reliability, maintainability, supportability and quality can provide the basis for developing a new paradigm in corrosion prevention and control. With such a broad charter and insight into the product life cycle, the reliability community can become the mechanism for breaking down the stovepipes that have long hindered the employment of existing corrosion-related technology. The challenge in transforming from current practice will be to take the skills, techniques and knowledge available from the materials community and convert them into a form that can be employed within the framework of current reliability practice.

Vision and Advocacy

As a leader in the reliability community, the RIAC has already taken significant steps towards developing a cross-functional approach towards corrosion prevention and control. The RIAC actively helped plan for, and subsequently participated in the recent Corrosion Education Workshop at the National Academies, where the author also presented a paper proposing, in part, that nontraditional stakeholders, including the reliability engineering community, could play a crucial role towards solving the corrosion problem. The initiative described in this article expands upon the subject discussed in this presentation.

At present, RIAC is beginning the process of engaging other entities within the reliability community to help solve the corrosion problem. As a first step, RIAC has contacted organizers of the international Reliability and Maintainability Symposium (RAMS) and proposed using this annual event as a venue for improving consideration and analysis of corrosion by reliability engineers. There are a number of other conferences and symposia that could be similarly engaged. The people responsible for both organizing these various reliability-oriented conferences/symposia and coordinating with the professional societies that sponsor them, are all senior members of the reliability community. Having them become advocates for the transformation proposed here will go far towards having the community become the standard bearer for improved CP&C practices.

Enhancing current reliability practices so that they comprehensively consider corrosion will require the community to build and maintain a certain degree of technological momentum. A well constructed strategic program to develop the initial complement of reliability-centric corrosion engineering tools and supporting data in conjunction with an outreach program designed to educate the community on the newly developed capabilities will be essential to develop this momentum. As the community begins to recognize the value of helping to control corrosion and subsequently employs the new tools and associated methodologies, individuals will recognize opportunities to evolve the initial tools into more mature approaches, methodologies, and other facilitators of the concepts. By sponsoring sessions dedicated to the development and maturation of these tools, the reliability-oriented conferences and symposia would become the mechanism to institutionalize the proposed transformation.

Phased Program to Transform CP&C Practices

A phased, four-pronged approach specifically designed to substantially reduce DoD’s corrosion costs through improved reliability practices is proposed here.

- The first task will be to conduct a workshop to assemble senior representatives from the reliability community so they can attain the insight and enthusiasm needed to subsequently advocate the process of transformation.
- The second task will be to convene an interdisciplinary working group that will develop the initial methodologies needed so that the reliability community can take on a greater role in preventing and controlling corrosion.
- The third task will be to develop an on-line knowledgebase of corrosion information aimed specifically towards the newly developed reliability-centric CP&C tools and processes.
- The final task will be to advocate and promote the output from these initial transformational activities.

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Conduct a Workshop

Currently, there is little general awareness concerning the magnitude of the corrosion problem within the broader engineering community. The National Association of Corrosion Engineers (NACE) has long been an effective resource for its own community and has done a good job at educating its membership. However, since the individual technical communities concerned with reliability or design will always gravitate towards the society aligned with their specific technology interests, it’s unlikely that NACE could unilaterally advocate and support a broader customer base. Therefore, we feel that comprehensively solving the corrosion problem will take a broader, more strategic approach.

A workshop attended by representatives of the organizing bodies for the reliability and design oriented conferences/symposia, along with the professional societies that sponsor them, could be the seminal event responsible for implementing a new, broad-based approach to corrosion prevention and control. Attendees at this workshop, for example, could include the organizers for RAMS, the Applied Reliability Symposium, the International Reliability Physics Symposium, the DoD Maintenance Symposium, and the Quality Congress. In addition, representatives from the American Institute for Aeronautics and Astronautics (AIAA), the American Society for Quality (ASQ), the Institute of Electrical and Electronics Engineers (IEEE), the Institute of Environmental Sciences and Technology (IEST), the Institute of Industrial Engineers (IEE), the Society of Automotive Engineers (SAE), the Society of Logistics Engineers (SOLE), the Society of Reliability Engineers (SORE), the System Safety Society (SSS), and the American Society for Mechanical Engineers (ASME) could also attend. This workshop could commence by having presentations by Government officials and authors of the report that contains the results from the Government-sponsored “cost of corrosion” study. It would then conclude with additional presentations and panel discussions. This proposed event could very well become the mechanism for energizing the societies (and the events they sponsor) and get them to cooperatively work together as a community to implement a comprehensive approach towards improving CP&C practices.

Developing Initial Reliability-Centric CP&C Processes

To support the above efforts and jump-start the transformation within the reliability community, an interdisciplinary working group of reliability, design, and materials engineers would be convened by RIAC to examine existing reliability practices and determine which ones would best form the basis for new reliability-focused corrosion prevention and control analysis methods. Some initial candidates that immediately come to mind include failure modes and effects analysis (FMEA), failure modes, effects and criticality analysis (FMECA), fault tree analysis (FTA), and review of mechanical designs through the use of checklists. However, there are certainly many other existing practices that could also form the basis for new reliability-centric corrosion prevention and control processes. The working group could then examine the CP&C methodologies developed by the materials community as they modify existing reliability methodologies to implement the initial suite of reliability-centric corrosion management methodologies.

With proper advocacy and coordination, the new reliability-centric CP&C processes discussed above can become well recognized and institutionalized analysis methodologies, especially if they are adopted by the American Society for Quality’s (ASQ) reliability certification program. The ASQ CRE program could become the mechanism to ensure that the reliability community maintains the long-term focus needed for it to become a critical stakeholder in CP&C.

Advocate and Promote the New Reliability Processes and Resources

A key factor necessary to ensure that this initiative succeeds is to actively promote the new reliability analysis methods to the intended user community. To initiate these transformation efforts, the RIAC will actively coordinate our activities with organizers from the various reliability-oriented conferences/symposia. This coordination is vitally important to ensure that platforms exist for promoting the newly developed reliability-centric corrosion prevention and control analysis methods. Some initial candidates that immediately come to mind include failure modes and effects analysis (FMEA), failure modes, effects and criticality analysis (FMECA), fault tree analysis (FTA), and review of mechanical designs through the use of checklists. However, there are certainly many other existing practices that could also form the basis for new reliability-centric corrosion prevention and control processes. The working group could then examine the CP&C methodologies developed by the materials community as they modify existing reliability methodologies to implement the initial suite of reliability-centric corrosion management methodologies.

Not only do we plan on engaging conference/symposia organizers so that they will host corrosion-related sessions at their annual events, we will also advocate emerging analysis methods by authoring and presenting technical papers. This article is a start, and an abstract for a similar, but more comprehensive, paper describing the proposed transformation and the opportunity it represents has already been submitted for RAMS 2008. We will also leverage RIAC’s traditional DoD-funded current awareness program by publishing future RIAC Journal articles to promote awareness of new analysis techniques, training opportunities and data products. Since the RIAC Journal reaches such a broad cross-section of the reliability community, it should be a particularly effective mechanism for getting out the word. RIAC will also use its web site, its frequently emailed technology briefs, and its reliability engineering training programs to institutionalize the concepts.
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He has been the principal advocate for improving corrosion education within undergraduate engineering curricula at our nation’s colleges and universities, first presenting his vision on undergraduate education to the Defense Science Board’s Corrosion Task Force. He subsequently briefed congressional staffers supporting the Senate Armed Services Committee and convinced them of the need for a DoD-sponsored study by the National Academies to investigate corrosion education and make recommendations on the measures that engineering colleges and universities could implement to revise their curricula. He helped organize, and presented at, the workshop kicking off this ongoing study. His presentation included discussion on how nontraditional stakeholders such as the reliability community could play a critical role in corrosion prevention and control.

This RIAC Journal article begins the formal dialog on this idea and presents an approach for how the reliability community can unite and cooperatively implement measures to help solve this critical problem.

If you or your organization are interested in getting involved in this strategic initiative to develop and promote new capabilities within the reliability engineering discipline, please contact:

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Material scientists, device technologists, and microwave designers must focus on the reliability concerns of the products which are being developed from compound semiconductor structures.

The book focuses on a physics of failure approach to the understanding of MMIC reliability, covering basic failure modes for each of the device building blocks, up to packaged MMIC modules.

This book will allow the GaAs technologist, designer and graduate student to become familiar with the issues related to product reliability and to develop the reliability prediction tools which ensure that reliability and performance margins are designed into each product.
On 29 July 2003, the Office of the Under Secretary of Defense for Acquisition, Technology and Logistics issued a policy memo stating that every individual DoD part valued at over $5K, or meeting certain other criteria, would have to have a unique identification number [Reference 1]. This serial number would have to be marked on a label or data plate, or on the part itself, in the form of a Data Matrix 2-dimensional barcode. New parts would get this 2D barcode applied during their manufacture. Existing parts not already marked would get this barcode applied during their regularly scheduled maintenance at a depot. This policy is known as Unique Identification, or UID. To comply with the UID policy, DoD depot maintenance activities had to determine the impact of this policy on their operations and make plans to implement the policy. Implementation of UID at a depot involves such things as the purchase of appropriate equipment and services, the writing and modifying of procedures, and the training of personnel. The Applied Research Laboratory at Penn State University assisted the Navy and Marines Corps depot maintenance activities in their UID planning by identifying the tasks to be carried out and estimating the costs involved in implementing UID at depots and shipyards. This UID Depot Implementation Study was sponsored by the Office of Naval Research (ONR) Repair Technology Program (RepTech).

Currently, there are eleven Navy and Marines Corps depot maintenance sites in the U.S. These sites consist of four Naval Sea Systems Command (NAVSEA) Naval Shipyards, two NAVSEA Warfare Center depots, three Naval Air Systems Command (NAVAIR) aviation depots, and two Marine Corps logistics bases. For this study, data was collected at four representative sites out of the eleven total sites. The UID implementation tasks that are included in this study are limited to those tasks that will have to be carried out at the depots by depot personnel. In addition to these tasks, there are many other UID-related tasks that must be carried out by other DoD organizations to complete the overall implementation of UID. The UID implementation costs estimated in this study are only those costs incurred by the depots in carrying out their UID-related tasks.

UID Background

“UID” stands for Unique Identification. The UID is a serial number that distinguishes one item from another, even within a group of like items (items with the same Part Number). The purpose of the UID program is to enable the DoD to achieve Total Asset Visibility, improved item management, and clean financial audits for DoD property by tracking items via their UIDs. The UID enables an individual item to be tracked as it moves from place to place and progresses through acquisition, storage, operation, maintenance and, finally, disposal. The major focus of UID item tracking is on an item’s location, operational status, maintenance history and value. The UID policy memo lists the criteria for those items that require UIDs (UID-qualifying items). A UID-qualifying item can be a component part, an assembly, or an end item.

The UID serial number is a globally unique string with a maximum length of 78 characters. The allowable characters are uppercase letters A-Z, numbers 0-9, and the symbols “/” and ““. The UID serial number must be marked on an item in the form of a machine-readable, 2-dimensional Data Matrix ECC 200 barcode symbol like the one shown in Figure 1. The UID characters are encoded in the checkerboard pattern of light and dark squares. These symbols are read and decoded using special optical 2D barcode readers.

The UID symbol must be applied to an item in such a way that it can survive the item’s normal operating conditions.

Figure 1: 2D Data Matrix ECC 200 Barcode
The UID symbol can be marked on a label or data plate that is affixed to the item, or it can be marked directly on the item. This second method is referred to as direct part marking. The primary marking technologies used in direct part marking are dot peening, electro-chemical etching, laser marking and inkjet marking.

The selection of a direct part marking method for a part depends on the material being marked, the size, shape, and color of the surface to be marked, the production volume, the marking environment, and the conditions the part will see during its lifecycle. The engineering authority for a part will determine the marking method to be used to apply the UID to that part. Since the depots will likely be called upon to mark parts using all four of the direct part marking methods mentioned above, the UID marking stations recommended for the depots in this study have all four types of direct part marking equipment. Figure 2 shows photos of a Marine Corps 7½ ton crane and its associated data plate with UID.

When a UID-marked item is first received by the DoD, an initial set of data is collected and stored under the item’s UID number. This initial set of data is stored in a DoD database called the UID Registry. The UID Registry is the master database containing all the UID serial numbers issued along with their initial sets of data, or “birth records”. The 18 data elements that comprise the birth record for a UID-marked part are as follows:

1. Item Description
2. Unique Identification
3. Unique item identifier type
4. Issuing agency code
5. Enterprise identifier
6. Lot or batch number
7. Original part number
8. Current part number
9. Current part number effective date
10. Serial number
11. Unit of measure
12. Government’s unit acquisition cost
13. Ship-to code
14. Contractor’s CAGE code or DUNS number
15. Contract number
16. Contract line, subline, or exhibit line item number
17. Acceptance code
18. Shipment date

Figure 2: Marine Corps 7½ Ton Crane with UID Symbol on Data Plate

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The activity that first receives a UID-marked item will be responsible for entering the item’s UID and initial set of data into the UID Registry.

**UID Implementation at Navy and Marine Corps Depots**

The UID policy affects all eleven Navy/Marine Corps depot maintenance activities, which are listed below:

- **NAVSEA**
  - Norfolk NSY (participating site)
  - Portsmouth NSY
  - Pearl Harbor NSY
  - Puget Sound NSY
  - NUWC Keyport depot (participating site)
  - NSWC Crane depot
- **NAVAIR**
  - NADEP Cherry Point (participating site)
  - NADEP Jacksonville
  - NADEP North Island
- **USMC**
  - MC Barstow (participating site)
  - MC Albany

Four “representative” sites were chosen from the eleven to provide data for the study. Each of the four participating sites represents one of the four categories of Navy/Marine Corps depot maintenance activities: one NAVSEA Naval Shipyard (NSY), one NAVSEA Warfare Center depot, one NAVAIR Naval Aviation Depot (NADEP), and one Marine Corps Maintenance Center. The sites selected were: Norfolk Naval Shipyard (Norfolk NSY), Naval Aviation Depot Cherry Point (NADEP Cherry Point), Naval Undersea Warfare Center Keyport (NUWC Keyport), and Marine Corps Maintenance Center Barstow (MC Barstow). The UID implementation costs calculated for the four participating sites can be used to estimate the costs at the other sites, based on their relative sizes and workloads compared to the participating sites.

There are many places at a depot where a UID symbol must be either marked on a part or read from a part in order to track that part in compliance with the UID policy. Listed below are the areas at a depot where UID-related activities will likely take place, and a brief explanation of the UID-related tasks and equipment in those areas:

**Shipping/Receiving** – When an item with a UID symbol enters or leaves the depot, the UID must be read and the appropriate tracking database must be updated to reflect the item’s current location and condition. UID readers should be stationed in this area to capture the UID data as an item enters or leaves the depot.

**Disassembly/Reassembly** – When an assembly has a UID symbol, and some of its embedded component parts also have UID symbols, the tracking database for those items will contain parent-child relationships that link the components to the assembly. When UID-marked component parts are either removed from or added to an assembly, the parent-child links must be updated in the tracking database. UID readers should be stationed in the disassembly and reassembly areas to capture the UID numbers of the parent and child items.

**Maintenance/Repair/Overhaul** – There are many UID-qualifying parts currently in the supply system that do not yet have UID symbols marked on them. It will be the responsibility of the depots to markUIDs on these parts when they come through for regular scheduled maintenance. In the areas of a depot where this work takes place; there will need to be UID marking equipment, verifiers, and readers in order to carry out the task of marking legacy items and entering the required data into the UID Registry.

**Manufacturing** – Some depots manufacture spare parts from raw stock for use in overhauling or repairing weapons systems. If any of these manufactured spare parts are UID-qualifying, then the depots will have to mark UID symbols on them. To do this, the depots will need to have UID marking, verifying, and reading equipment in those areas where spare parts are manufactured from raw stock.

**Cleaning** – Some depots have powerful cleaning operations that strip material from parts. Examples are grit blasting and acid washing. Operations such as these could possibly remove an existing UID symbol from a part. If, after the cleaning operation, the original UID is gone, then the same UID number must be re-marked on the part so that the part retains its original serial number. For this reason, a depot must have UID marking and reading equipment in those areas where powerful part cleaning operations take place.

**Scrap** – Depots occasionally scrap items that are obsolete or too damaged to be repairable. If such a part has a UID symbol on it, then the depot must update the tracking database to reflect the disposal of the part. UID readers should be stationed in those areas where the disposal of scrap items takes place.
UID Implementation Costs

To implement the UID policy, depots will incur costs in several areas. UID-related equipment will have to be procured and maintained, documents and work instructions will have to be written, personnel will have to be trained, and the tasks of marking and reading UID symbols on parts will have to be carried out. In addition to marking UID symbols on weapons systems parts and assemblies that come to the depots for maintenance, depots will also have to mark UIDs on their own industrial plant equipment (IPE). There are costs associated with each of these task areas. The costs in these areas may have both nonrecurring and recurring components. The nonrecurring costs are the initial costs that are incurred once, usually at startup. The recurring costs are costs associated with UID that are incurred continually as UID tasks are performed. In this study, recurring costs are expressed on a per-year basis. Table 1 defines the UID implementation cost categories and tasks, divided into their nonrecurring and recurring components.

Data

For this study, data was needed in order to calculate costs for the implementation tasks listed above. Most of the required data was available from the sites that participated in the study. Additional data, such as prices for UID equipment, was obtained from vendors. The labor times required to mark, read and verify UID symbols on parts were determined by actually measuring the time it took to mark, read and verify symbols on a variety of sample parts using real UID equipment.

In the Equipment category, there are costs to procure UID equipment (nonrecurring cost) and maintain UID equipment (recurring cost). UID equipment includes marking equipment, reading equipment and verifying equipment. To calculate these costs, data was collected on the numbers of each type of equipment, their prices and their maintenance costs. The appropriate numbers of marking stations, readers and verifiers were determined for each site in the study. Prices for each type of equipment were obtained from vendors. The price for a complete marking station, including equipment for all four types of direct part marking, was approximately $200,000. The price for an optical reader was $5,000, and the price for a complete laboratory-type verifier was $10,000. Suggested maintenance policies and costs were obtained from vendors and experienced users of UID equipment.

To calculate Documentation costs, data was collected at the depots on the number of documents that would need to be written or revised to include UID. The man-hours required to write or revise the documents was also determined. A standard burdened labor rate of $100/hour was used in this and all other labor cost calculations.

In the Training category, data was collected at each site on the number of people to be trained in UID marking, reading and verifying. The costs and duration of training classes were obtained from UID equipment vendors.

The costs for marking, reading and verifying UIDs on Industrial Plant Equipment and regular Depot Maintenance Workload were calculated from the number of items, the labor time and the labor rate. Workload numbers were supplied by each site in the study. Average times required to mark, read, and verify a UID were calculated through experimentation using actual UID equipment. The standard burdened labor rate of $100/hour was used in the cost calculations.

Table 1: Depot Implementation Cost Categories and Tasks

<table>
<thead>
<tr>
<th>Cost Category</th>
<th>Description of Tasks</th>
</tr>
</thead>
<tbody>
<tr>
<td>Equipment</td>
<td>Procurement of UID marking, reading, and verifying equipment</td>
</tr>
<tr>
<td></td>
<td>Maintenance of UID marking, reading, and verifying equipment</td>
</tr>
<tr>
<td>Documentation</td>
<td>One-time development or revision of drawings, procedures, work instructions, etc. to include UID requirements</td>
</tr>
<tr>
<td></td>
<td>Ongoing development or revision of drawings, procedures, work instructions, etc. to include UID requirements</td>
</tr>
<tr>
<td>Training</td>
<td>Initial employee training in UID</td>
</tr>
<tr>
<td></td>
<td>Refresher employee training in UID</td>
</tr>
<tr>
<td>Industrial Plant Equipment</td>
<td>Labor to mark existing depot industrial plant equipment</td>
</tr>
<tr>
<td></td>
<td>Labor to mark newly-acquired depot industrial plant equipment</td>
</tr>
<tr>
<td>Depot Maintenance Workload</td>
<td>N/A</td>
</tr>
<tr>
<td></td>
<td>Labor to mark, read, and verify UIDs on items flowing through the depot as part of regular depot workload</td>
</tr>
</tbody>
</table>
IMPLEMENTING UNIQUE IDENTIFICATION (UID) AT DEPOT MAINTENANCE ACTIVITIES
continued from page 9

Results

One of the first steps in planning for UID implementation at a depot maintenance activity is to understand the costs involved. As stated earlier, these costs include investment costs in equipment, documentation and training, as well as ongoing costs for equipment maintenance, new documentation revisions, refresher training and regular depot workload.

In the category of Equipment, the cost to procure the necessary UID equipment for a depot ranged from $1.7M for the smallest depot to over $8M for the largest. This assumed that each site would purchase enough equipment so that material could still flow smoothly through the depot without a lot of extra material handling. This meant placing the marking stations, readers and verifiers in strategic locations, close to where UID-marked items are normally worked on. The recurring costs for UID equipment includes the annual cost of consumables used by the equipment and the annual cost of maintenance. For any given site, this cost is a function of the number of pieces of UID equipment at the site. The costs ranged from $140,000 per year for the smallest depot to almost $800,000 per year for the largest.

In the Documentation category, most sites had only a nonrecurring cost. That was the cost to write or revise any documents at the depot that would need to call out UID-related specifications or instructions. Normally these documents would only need to be written or revised once. For shipyards, which produce new documents every time a ship comes in for maintenance, there is also a recurring documentation cost. The cost to a depot of changing documentation relevant to UID is dependent upon how many
documents that site is responsible for. Two of the sites in this study maintained several hundred or fewer documents affected by UID. These sites had one-time documentation costs of around $100,000. The other two sites had maintenance responsibility for several thousand or more documents that would be affected by UID. The costs to write or revise these documents amounted to over $10M per site. In addition, the shipyard has recurring documentation costs totaling several million dollars per year.

For Training, each site’s cost is a function of the number of people to be trained at the site. Most depots will train fewer than 50 people in UID marking and verifying, but may train several hundred or several thousand in UID reading. For the sites in this study, the initial cost of UID training for the workforce ranged from $200,000 to $900,000. Refresher training ranged from $40,000 to $200,000 annually.

The cost to mark Industrial Plant Equipment (IPE) at a site was dependent upon the number of pieces of IPE at the site. The sites in this study averaged about $100,000 to mark their current IPE inventory and less that $10,000 per year to mark newly-acquired IPE.

The cost to mark and read UIDs on items in a depot’s normal workload is a function of the depot’s workload volume. Sites that handle large numbers of UID-qualifying items will have higher costs in this category than sites with smaller workloads. The UD implementation costs in the Depot Maintenance Workload Category are recurring costs. In this study, those costs ranged from under $100,000 per year for the depot with the smallest workload to over $3M per year for the depot with the largest workload.

In total, the nonrecurring costs for the four sites in this study ranged between $2M and $22M, and recurring costs varied between $0.5M and $4M per year.

As with many new technologies, the implementation of UID at Depot maintenance activities will require a significant investment in new equipment, documentation and training. In addition, there will be the ongoing costs of carrying out UID-related tasks such as marking UIDs on items, reading UIDs on items, and entering data into databases to track those items. Implementing the UID policy throughout the DoD will not be cheap. However, it is expected that the benefits derived from UID will outweigh the costs.

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References

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THE RIAC 217PLUS™ CAPACITOR AND DIODE FAILURE RATE MODELS

David Nicholls, RIAC (Quanterion Solutions Incorporated)

In the First Quarter 2007 issue of the RIAC Journal [Reference 1], I provided a high-level introduction to the 217Plus™ component failure rate prediction models. I first defined the overall 217Plus™ system reliability assessment model:

$$\lambda_P = \lambda_{IA} (\Pi_P + \Pi_D + \Pi_W + \Pi_S + \Pi_I + \Pi_N + \Pi_M) + \lambda_{SW}$$

where,

- $\lambda_P$ = Predicted failure rate of the system
- $\lambda_{IA}$ = Initial assessment of failure rate from 217Plus™ failure rate models/data
- $\Pi_P$ = Parts process multiplier
- $\Pi_D$ = Design process multiplier
- $\Pi_W$ = Manufacturing process multiplier
- $\Pi_S$ = System Management process multiplier
- $\Pi_I$ = Induced process multiplier
- $\Pi_N$ = No defect process multiplier
- $\Pi_M$ = Wearout process multiplier
- $\lambda_{SW}$ = Software failure rate prediction

Next, I introduced the basic form and rationale behind the 217Plus™ component reliability models and how they contribute to the initial assessment of the system failure rate, $\lambda_{IA}$, which serves as the seed failure rate value for the system model defined above. The generic component reliability model was defined as:

$$\lambda_P = \lambda_o \pi_o + \lambda_e \pi_e + \lambda_c \pi_c + \lambda_i + \lambda_{sj} \pi_{sj}$$

where,

- $\lambda_P$ = Predicted failure rate of the system
- $\lambda_o$ = Failure rate from operational stresses
- $\pi_o$ = Parts process multiplier
- $\lambda_e$ = Failure rate from environmental stresses
- $\pi_e$ = Product of failure rate multipliers for environmental stresses
- $\lambda_c$ = Failure rate from power or temperature cycling stresses
- $\pi_c$ = Product of failure rate multipliers for cycling stresses
- $\lambda_i$ = Failure rate from induced stresses, including EOS and ESD
- $\lambda_{sj}$ = Failure rate from solder joints
- $\pi_{sj}$ = Product of failure rate multipliers for solder joint stresses

The twelve component models contained within the current 217Plus™ methodology are:

- Capacitors
- Connectors
- Diodes
- Inductors
- Integrated Circuits
- Optoelectronic Devices
- Relays
- Resistors
- Switches
- Thyristors
- Transformers
- Transistors

Beginning with this issue of the RIAC Journal, I will begin to present the individual component models in their entirety, starting with the 217Plus™ capacitor and diode models. A brief example will be provided at the end of the article.

217Plus™ Capacitor Failure Rate Model

The failure rate equation for capacitors [Reference 2] is:

$$\lambda_P = \pi_o \lambda_c (\lambda_{EC} \pi_{CE} \pi_{CS} + \lambda_{ES} \pi_{CE} \pi_{ES} + \lambda_{SW} \pi_{CE} \pi_{SW} + \lambda_{SE} \pi_{CE} \pi_{SE} + \lambda_{SO} \pi_{CE} \pi_{SO} + \lambda_{SD} \pi_{CE} \pi_{SD})$$

where,

- $\lambda_P$ = Predicted failure rate in failures per million calendar hours
- $\pi_o$ = Reliability growth failure rate multiplier:
  $$\pi_c = e^{-\beta (y - 1993)}$$
- $\beta$ = Growth constant. Function of capacitor type (see Table 1)
- $\pi_c$ = Capacitance failure rate multiplier:
  $$\pi_c = \left(\frac{C}{C_i}\right)^{CE}$$
  $C_i$ = Capacitance, in microfarads
  $C_i$ = Constant. Function of capacitor type (see Table 1)
  $CE$ = Constant. Function of capacitor type (see Table 1)
\( \lambda_{OB} \) = Base failure rate, operating. Function of capacitor type (see Table 1)

\( \pi_{DCO} \) = Failure rate multiplier for duty cycle, operating:

\[
\pi_{DCO} = \frac{DC}{DC_{\text{op}}}
\]

\( DC_{\text{op}} \) = Constant. Function of capacitor type (see Table 1)

\( \pi_{TO} \) = Failure rate multiplier for temperature, operating:

\[
\pi_{TO} = e^{-\frac{E_{op}}{k \cdot T_{AO}}}
\]

\( E_{op} \) = Activation energy, operating. Function of capacitor type (see Table 1)

\( \pi_{S} \) = Failure rate multiplier for stress:

\[
\pi_{S} = \left( \frac{S_{A}}{S_{1}} \right)^{n}
\]

\( S_{A} \) = Stress ratio, the applied voltage stress divided by the rated voltage

\( S_{1} \) = Constant. Function of capacitor type (see Table 1)

\( n \) = Constant. Function of capacitor type (see Table 1)

\( \lambda_{EB} \) = Base failure rate, environmental (see Table 1)

\( \pi_{DCN} \) = Failure rate multiplier, duty cycle - nonoperating:

\[
\pi_{DCN} = \left( 1 - \frac{DC}{DC_{\text{onop}}} \right)
\]

\( DC_{\text{onop}} \) = Constant. Function of capacitor type (see Table 1)

\( \pi_{TE} \) = Failure rate multiplier, temperature - environment:

\[
\pi_{TE} = e^{-\frac{E_{nonop}}{k \cdot T_{AE}}}
\]

\( E_{nonop} \) = Activation energy, nonoperating. Function of capacitor type (see Table 1)

\( \lambda_{TCB} \) = Base failure rate, temperature cycling (see Table 1)

\( \pi_{CR} \) = Failure rate multiplier, cycling rate:

\[
\pi_{CR} = \frac{CR}{CR_{1}}
\]

\( CR_{1} \) = Constant. Function of capacitor type (see Table 1)

\( \pi_{DT} \) = Failure rate multiplier, delta temperature:

\[
\pi_{DT} = \left( \frac{T_{AO} - T_{AE}}{DT_{1}} \right)^{2}
\]

\( DT_{1} \) = Constant. Function of capacitor type (see Table 1)

\( \lambda_{SJ} \) = Base failure rate, solder joint (see Table 1)

\( \pi_{SDT} \) = Failure rate multiplier, solder joint delta temperature:

\[
\pi_{SDT} = \left( \frac{T_{AO} - T_{AE}}{44} \right)^{2.26}
\]

\( \lambda_{IND} \) = Failure rate, induced (see Table 1)

NOTE: Environment-type and equipment-dependent default values for DC, TAO, TAE, and CR were previously presented in Reference 3, where:

DC = Duty cycle (the percent of calendar time that the system in which the component is operating is in an operational state)

TAO = Ambient temperature, operating (in degrees C)

TAE = Ambient temperature, nonoperating (in degrees C)

CR = Cycling rate (the number of power cycles per year to which the system is exposed). In this case, it is assumed that the system transitions from a nonoperating environment to an operating environment at the same time that the power is applied.
Table 1: Capacitor Parameters

<table>
<thead>
<tr>
<th>Part Type</th>
<th>$\lambda_{\text{OB}}$</th>
<th>$\lambda_{\text{EB}}$</th>
<th>$\lambda_{\text{TCB}}$</th>
<th>$\lambda_{\text{IND}}$</th>
<th>$\beta$</th>
<th>$E_{\text{DC}_{\text{op}}}$</th>
<th>$T_{\text{Refault}}$</th>
<th>$D_{\text{CALIB}}$</th>
<th>$E_{\text{CALIB}}$</th>
<th>$C_{\text{R}}$</th>
<th>$D_{T}$</th>
<th>$n$</th>
<th>$C_{1}$</th>
<th>$S_{1}$</th>
<th>$CE$</th>
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<td>Aluminum</td>
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<td>0.000214</td>
<td>0.000768</td>
<td>0.229</td>
<td>0.17</td>
<td>0.5</td>
<td>0.83</td>
<td>0.4</td>
<td>1140.35</td>
<td>21</td>
<td>5</td>
<td>7.6</td>
<td>0.6</td>
<td>0.23</td>
</tr>
<tr>
<td>Ceramic</td>
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<td>0.83</td>
<td>0.3</td>
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<td>21</td>
<td>3</td>
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<td>0.09</td>
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<tr>
<td>General</td>
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<td>0.000083</td>
<td>0.000259</td>
<td>0.033</td>
<td>0.17</td>
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<td>0.83</td>
<td>0.3</td>
<td>1140.35</td>
<td>21</td>
<td>7</td>
<td>0.1</td>
<td>0.6</td>
<td>0.09</td>
</tr>
<tr>
<td>Mica/Glass</td>
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<td>0.000997</td>
<td>0.000888</td>
<td>0.000764</td>
<td>0.0085</td>
<td>0.17</td>
<td>0.4</td>
<td>0.83</td>
<td>0.4</td>
<td>1140.35</td>
<td>21</td>
<td>10</td>
<td>0.1</td>
<td>0.6</td>
<td>0.09</td>
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<td>21</td>
<td>5</td>
<td>0.1</td>
<td>0.6</td>
<td>0.09</td>
</tr>
<tr>
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<td>0.83</td>
<td>0.2</td>
<td>1140.35</td>
<td>21</td>
<td>6</td>
<td>0.1</td>
<td>0.6</td>
<td>0.09</td>
</tr>
<tr>
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<td>0.0085</td>
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<td>0.83</td>
<td>0.2</td>
<td>1140.35</td>
<td>21</td>
<td>17</td>
<td>7.6</td>
<td>0.6</td>
<td>0.23</td>
</tr>
<tr>
<td>Variable, Air</td>
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<td>0.005193</td>
<td>0.002066</td>
<td>0.000566</td>
<td>0.0085</td>
<td>0.17</td>
<td>0.3</td>
<td>0.83</td>
<td>0.3</td>
<td>1140.35</td>
<td>21</td>
<td>6</td>
<td>0.35</td>
<td>0.5</td>
<td>0.09</td>
</tr>
<tr>
<td>Variable, Ceramic</td>
<td>0.002683</td>
<td>0.005193</td>
<td>0.002066</td>
<td>0.000566</td>
<td>0.0085</td>
<td>0.17</td>
<td>0.3</td>
<td>0.83</td>
<td>0.1</td>
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<td>21</td>
<td>3</td>
<td>0.35</td>
<td>0.5</td>
<td>0.09</td>
</tr>
<tr>
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<td>0.005193</td>
<td>0.002066</td>
<td>0.000566</td>
<td>0.0085</td>
<td>0.17</td>
<td>0.3</td>
<td>0.83</td>
<td>0.2</td>
<td>1140.35</td>
<td>21</td>
<td>6</td>
<td>0.35</td>
<td>0.5</td>
<td>0.09</td>
</tr>
<tr>
<td>Variable, General</td>
<td>0.002683</td>
<td>0.005193</td>
<td>0.002066</td>
<td>0.000566</td>
<td>0.0085</td>
<td>0.17</td>
<td>0.3</td>
<td>0.83</td>
<td>0.2</td>
<td>1140.35</td>
<td>21</td>
<td>6</td>
<td>0.35</td>
<td>0.5</td>
<td>0.09</td>
</tr>
<tr>
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<td>0.002683</td>
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<td>0.0085</td>
<td>0.17</td>
<td>0.3</td>
<td>0.83</td>
<td>0.2</td>
<td>1140.35</td>
<td>21</td>
<td>3</td>
<td>0.35</td>
<td>0.5</td>
<td>0.09</td>
</tr>
<tr>
<td>Variable, Plastic</td>
<td>0.002683</td>
<td>0.005193</td>
<td>0.002066</td>
<td>0.000566</td>
<td>0.0085</td>
<td>0.17</td>
<td>0.3</td>
<td>0.83</td>
<td>0.2</td>
<td>1140.35</td>
<td>21</td>
<td>10</td>
<td>0.35</td>
<td>0.5</td>
<td>0.09</td>
</tr>
</tbody>
</table>

217Plus™ Diode Failure Rate Model

The failure rate equation for diodes [Reference 2] is:

\[
\lambda = \pi_G (\lambda_{\text{B}} + \lambda_{\text{EB}} + \lambda_{\text{TCB}} + \lambda_{\text{IND}} + \lambda_{\text{DB}} + \lambda_{\text{T}})
\]

where,

- $\lambda_G$ = Predicted failure rate in failures per million calendar hours
- $\pi_G$ = Reliability growth failure rate multiplier:
  \[
  \pi_G = e^{\left(\beta \left(\frac{1 - \pi_{\text{DCO}}}{1 - \pi_{\text{DC}}}ight)\right)}
  \]
- $\beta$ = Growth constant. Function of diode type (see Table 2)
- $\lambda_{\text{OB}}$ = Base failure rate, operating. Function of diode type (see Table 2)
- $\pi_{\text{DCO}}$ = Failure rate multiplier for duty cycle, operating:
  \[
  \pi_{\text{DCO}} = \frac{D_C}{D_{\text{CALIB}}}
  \]
- $D_{\text{CALIB}}$ = Constant. Function of diode type (see Table 2)
- $\pi_{\text{TO}}$ = Failure rate multiplier for temperature, operating:
  \[
  \pi_{\text{TO}} = e^{\left(-\frac{E_{\text{a}_{\text{op}}}}{k} \left(\frac{1}{T_{\text{CALIB}}} - \frac{1}{T_{\text{TO}}} \right) \right)}
  \]
- $E_{\text{a}_{\text{op}}}$ = Activation energy, operating. Function of diode type (see Table 2)
- $T_{\text{R}}$ = The junction rise above the ambient operating temperature ($T_{\text{CALIB}}$). The junction temperature is, therefore, $T_{\text{CALIB}} + T_{\text{R}}$. $T_{\text{R}}$ can be calculated in several ways:
  \[
  T_{\text{R}} = D_{\text{T}} - T_{\text{Refault}}
  \]
  \[
  T_{\text{R}} = D_{\text{T}} - T_{\text{Refault}}
  \]
  \[
  T_{\text{R}} = D_{\text{T}} - T_{\text{Refault}}
  \]
\[
T_R = \theta_{JA} \cdot P
\]
\(\theta_{JA}\) is the junction-to-ambient thermal impedance
\(P\) is the power dissipated by the diode in the application

\[
T_R = \theta_{JC} \cdot P
\]
\(\theta_{JC}\) is the junction-to-case thermal impedance
\(P\) is the power dissipated by the diode in the application

\[
T_R = \Delta T \cdot S
\]
\(\Delta T\) is the difference in junction temperature between no power dissipated and full power dissipated
\(S\) is the stress ratio, and is equal to the actual forward current divided by the rated forward current

\[\pi_s = \text{Failure rate multiplier, stress:}\]
\[\pi_s = \left(\frac{V}{V_0}\right)^{2.43} \cdot 0.185\]
\(V\) is applied voltage
\(V_0\) is rated voltage

\[\pi_s = \frac{\text{Voltage applied} - \text{reverse}}{\text{Voltage rated} - \text{reverse}}\]
The value for the \(V_s\) default can be found in Table 2

\(\lambda_{EB} = \text{Base failure rate, environmental (see Table 2)}\)
\(\pi_{DCN} = \text{Failure rate multiplier, duty cycle, nonoperating:}\)
\[\pi_{DCN} = \left(1 - \frac{DC}{DC_{\text{nonop}}}\right)\]
\(DC_{\text{nonop}} = \text{Constant. Function of diode type (see Table 2)}\)

\(\pi_{TE} = \text{Failure rate multiplier, temperature - environment:}\)
\[\pi_{TE} = e^{-\frac{Ea_{\text{nonop}}}{kT}}\]
\(Ea_{\text{nonop}} = \text{Activation energy, nonoperating. Function of diode type (see Table 2)}\)

\(\lambda_{TCB} = \text{Base failure rate, temperature cycling (see Table 2)}\)
\(\pi_{CR} = \text{Failure rate multiplier, cycling rate:}\)
\[\pi_{CR} = \frac{CR}{CR_i}\]

\(\lambda_{CR} = \text{Constant. Function of diode type (see Table 2)}\)
\(\pi_{DF} = \text{Failure rate multiplier, delta temperature:}\)
\[\pi_{DF} = \left(\frac{T_AO + T_R - T_{AE}}{DT_i}\right)^2\]
\(DT_i = \text{Constant. Function of diode type (see Table 2)}\)
\(\lambda_{SIDT} = \text{Failure rate multiplier, solder joint delta temperature:}\)
\[\lambda_{SIDT} = \left(\frac{T_AO + T_R - T_{AE}}{44}\right)^{2.26}\]

\(\lambda_{IND} = \text{Failure rate, induced (see Table 2)}\)

As with the capacitor model, the environment-type and equipment-dependent default values for \(DC, T_AO, T_{AE}\), and \(CR\) were previously presented in Reference 3.

Note that Table 2 appears on the next page.

### Example

What is the predicted failure rate of a 100pf fixed polystyrene (plastic) capacitor manufactured in 2006 that is rated at 160V and stressed in its circuit application at 40V. The capacitor operates in a “Ground, Mobile, Heavy-wheeled” vehicle with an assumed operating temperature of 55°C, a dormant temperature of 14°C and a relative humidity of 40%. The operating profile of the equipment is typical of military ground equipment, with a duty cycle of 45% and a cycling rate of 263 cycles per year.

The failure rate equation for capacitors [Reference 2] is:

\[\lambda_C = \pi_{DCN} \cdot \pi_{TE} \cdot \pi_{CR} \cdot \pi_{IND}\]

where,

\[\pi_{DF} = e^{(-\beta(y - 1993))} = 0.8989\]
where \(\beta = 0.0082\) (from Table 1) and \(Y = 2006\) (given)

\[\pi_{CR} = \left(\frac{C}{C_i}\right)^{CE} = 0.5370\]
\(C = 0.0001\) microfarads (given as 100pf)
\(C_i = 0.10\) (from Table 1)
\(CE = 0.090\) (from Table 1)

\(\lambda_{CR} = 0.000994\)
Table 2: Diode Parameters

<table>
<thead>
<tr>
<th>Part Type</th>
<th>$\lambda_{OB}$</th>
<th>$\lambda_{EB}$</th>
<th>$\lambda_{TCB}$</th>
<th>$\lambda_{IND}$</th>
<th>$\lambda_{SJB}$</th>
<th>$\beta$</th>
<th>$DC_{op}$</th>
<th>$Ea_{op}$</th>
<th>$T_{AO}$</th>
<th>$V_{AO}$</th>
<th>$DC_{nonop}$</th>
<th>$Ea_{nonop}$</th>
<th>$CR_1$</th>
<th>$DT_1$</th>
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<td>Current Regulator</td>
<td>0.00007269</td>
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<td>0.00164</td>
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<td>0.223</td>
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<td>60</td>
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<td>0.77</td>
<td>0.4</td>
<td>736.84</td>
<td>80</td>
</tr>
<tr>
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<td>0.000144</td>
<td>0.000629</td>
<td>0.0002</td>
<td>0.00365</td>
<td>0.000021</td>
<td>0.223</td>
<td>0.23</td>
<td>0.3</td>
<td>60</td>
<td>0.29</td>
<td>0.77</td>
<td>0.4</td>
<td>736.84</td>
<td>80</td>
</tr>
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<td>0.0000254</td>
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<td>0.02741</td>
<td>0.000021</td>
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<td>60</td>
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<td>0.77</td>
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<td>0.77</td>
<td>0.4</td>
<td>736.84</td>
<td>80</td>
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<td>0.000888</td>
<td>0.0019</td>
<td>0.00423</td>
<td>0.000021</td>
<td>0.223</td>
<td>0.23</td>
<td>0.3</td>
<td>60</td>
<td>0.29</td>
<td>0.77</td>
<td>0.4</td>
<td>736.84</td>
<td>80</td>
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<td>0.0001127</td>
<td>0.000608</td>
<td>0.000074</td>
<td>0.00316</td>
<td>0.000021</td>
<td>0.223</td>
<td>0.23</td>
<td>0.3</td>
<td>60</td>
<td>0.29</td>
<td>0.77</td>
<td>0.4</td>
<td>736.84</td>
<td>80</td>
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<td>0.000399</td>
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<td>0.0000037</td>
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<td>0.29</td>
<td>0.77</td>
<td>0.4</td>
<td>736.84</td>
<td>80</td>
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<td>0.0006</td>
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<td>0.3</td>
<td>60</td>
<td>0.29</td>
<td>0.77</td>
<td>0.4</td>
<td>736.84</td>
<td>80</td>
</tr>
<tr>
<td>Low Frequency, Bridge Rectifier</td>
<td>0.0001306</td>
<td>0.001589</td>
<td>0.00053</td>
<td>0.00295</td>
<td>0.000021</td>
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<td>60</td>
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<td>0.000098</td>
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<td>0.77</td>
<td>0.4</td>
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<td>60</td>
<td>0.29</td>
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<td>Low Frequency, Switching</td>
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<td>0.002748</td>
<td>0.02603</td>
<td>0.01158</td>
<td>0.000021</td>
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<td>0.3</td>
<td>60</td>
<td>0.29</td>
<td>0.77</td>
<td>0.4</td>
<td>736.84</td>
<td>80</td>
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<td>Low Frequency, Transient Suppressor</td>
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<td>0.001288</td>
<td>0.000048</td>
<td>0.0023</td>
<td>0.000021</td>
<td>0.15</td>
<td>0.23</td>
<td>0.3</td>
<td>60</td>
<td>0.29</td>
<td>0.77</td>
<td>0.3</td>
<td>736.84</td>
<td>80</td>
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<td>Low Frequency, Zener</td>
<td>0.0004102</td>
<td>0.000988</td>
<td>0.000032</td>
<td>0.00226</td>
<td>0.000021</td>
<td>0.15</td>
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<td>60</td>
<td>0.29</td>
<td>0.77</td>
<td>0.3</td>
<td>736.84</td>
<td>80</td>
</tr>
</tbody>
</table>

$\pi_{DCO} = \frac{DC}{DC_{nonop}} = 2.647$

$DC = 0.45$ (given as 45%)

$DC_{nonop} = 0.17$ (from Table 1)

$\pi_{TO} = e^{\frac{T_{AO}}{T_{AO} + 273}} = 2.039$

$Ea_{op} = 0.20$ (from Table 1)

$T_{AO} = 55$ (given)

$n = 6$ (from Table 1)

S_A = 0.25 (calculated from given)

S_i = 0.60 (from Table 1)

$\lambda_{EB} = 0.001462$ (from Table 1)

$\pi_{DCN} = \left(1 - \frac{DC}{DC_{nonop}}\right) = 0.6627$

$DC = 0.45$ (given as 45%)

$DC_{nonop} = 0.83$ (from Table 1)
\[ \pi_{TE} = e^{\left[-\frac{E_a_{\text{monop}}}{k}\left(\frac{1}{T_E} - \frac{1}{T_W}\right)\right]} = 0.7419 \]

\[ E_{a_{\text{monop}}} = 0.20 \text{ (from Table)} \]
\[ T_{AE} = 14 \text{ (given)} \]

\[ \lambda_{TCB} = 0.001657 \text{ (from Table 1)} \]

\[ \pi_{CR} = \frac{CR}{CR_1} = 0.2306 \]

\[ CR = 263 \text{ (given)} \]
\[ CR_1 = 1140.35 \text{ (from Table 1)} \]

\[ \pi_{DT} = \left(\frac{T_{AO} - T_{AE}}{DT_1}\right)^2 = 3.812 \]

\[ T_{AO} = 55 \text{ (given)} \]
\[ T_{AE} = 14 \text{ (given)} \]
\[ DT_1 = 21 \text{ (from Table 1)} \]

\[ \pi_{MIDT} = \left(\frac{T_{AO} - T_{AE}}{44}\right)^{2.26} = 0.8525 \]

\[ T_{AO} = 55 \text{ (given)} \]
\[ T_{AE} = 14 \text{ (given)} \]

Finally,

\[ \lambda_p = \frac{(0.8989)(0.5370)^*}{[(0.000994)(2.647)(2.039)(0.0052) + (0.001462)(0.6627)(0.7419) + (0.001657)(0.2306)(3.812)] + (0.00095)(0.8525) + (0.002531)} \]

\[ \lambda_p = 0.0044 \text{ f/10}^6 \text{ calendar hours} \]

In the Next Issue

The Third Quarter 2007 issue of the RIAC Journal will present the 217Plus\textsuperscript{TM} integrated circuit and inductor failure rate models in more detail.

References

1. “An Introduction to the RIAC 217Plus\textsuperscript{TM} Component Failure Rate Models”, Journal of the Reliability Information Analysis Center, First Quarter 2007, available for download from the RIAC at http://theRIAC.org

The appearance of paid advertising in the RIAC Journal does not constitute endorsement by the Department of Defense or the Reliability Information Analysis Center of the products or services advertised.
A thorough reliability investigation of pseudomorphic high
electron mobility transistors (pHEMTs) has been carried out
by investigating the effect on reliability of the active layer
dislocation density, interfacial defects and interfacial trap
centers. A mechanical stress characterization has been car-
rried out on the substrates prior to molecular beam epitaxy
(MBE) growth. The presence of thin (less that 200Å) lattice
mismatched pseudomorphic structures of InGaAs/AlGaAs
and InGaAs/GaAs may result in mechanical stress problems
which would limit the transistor’s reliability, even though
such a thickness may be at the critical length limits. The
present investigation reports on the reliability results of an
optimized doped channel heterojunction field effect transis-
tor (HFET) with a delta doped InGaAs channel of 1.5 x 10^{12}
cm^{-2}. The transistors were fabricated with a T-gate process
and with 0.25µm x 50µm TiPtAu gates.

Both the HEMT and the pHEMT degraded devices showed
the presence of a minority carrier trap of density greater than
10^{16} cm^{-3}. In addition, source resistance (R_s) for the HEMT
increased from a 1.25 Ω-mm to 4.5 Ω-mm, while for the
pHEMT, R_s increased from 1.45 Ω-mm to 2.7 Ω-mm. Since
the minority carrier trap identified was similar to the distri-
bution of traps present when the InGaAs layer creates dis-
locations, its presence after accelerated life testing has been
attributed to dislocations present at the InGaAs/GaAs inter-
face. The transmission electron microscopy (TEM) investiga-
tion showed the presence of two types of dislocations: Type
A was found to originate in the substrate and to propagate
by a climb mechanism to the active device layer. Type B was
generated at the InGaAs-GaAs interface and is due to thick-
ness variations resulting in a lack of strain accommodation.
In conclusion, the pseudomorphic layer of InGaAs has been
shown to contribute significantly to the degradation of In-
GaAs pHEMTs after accelerated life testing.

Previous investigations on the reliability of pHEMTs have
concentrated on the mechanisms of breakdown and device
instability. The review of the present understanding of
breakdown is given in Reference 1. As the requirement for
output voltage increases, devices biased to maximum volt-
age levels have shown a propensity to biased-induced insta-
bilities. This investigation reports that the dominant failure
mechanisms are due to defects (dislocations) generated at the
InGaAs-GaAs interface, and subsequent trapping and emis-
sion of carriers at such defect centers results in breakdown
instabilities.

**Experiment**

Electron beam lithographic techniques were used for gate-
lengths of 0.25µm. Figure 1 shows the cross-sections for both
the pHEMTs with the delta doped channel either in the AlGaAs
or InGaAs layer. The accelerated life tests were conducted at a
base plate temperature of 180˚C, 195˚C, 210˚C and 240˚C. The
following DC characteristics were measured before and after
accelerated stress testing: I_Ds - V_Gs behavior, transconduc-
tance (g_m), output conductance (g_0T), drain-gate breakdown
characteristics (BVDG), drain-source breakdown characteristics
(BVDS), threshold voltage, and saturated drain current (IDSS).
The transmission-technique was used to obtain specific con-
tact resistivity, transfer resistance and sheet resistance.

![Figure 1a: Cross-section of the pHEMT Showing the Placement of the Planar Doped Layer in the InGaAs Channel](image)

![Figure 1b: Cross-sections of Pseudomorphic InGaAs SHEMT](image)
The degradation was analyzed by deep level transient spectroscopy (DLTS) techniques and by cross-sectional transmission electron microscopy (TEM). DLTS techniques have been applied previously to HEMTs and have successfully reported on the presence of both minority and majority carrier traps due to accelerated stress testing. In addition, source resistance \( R_s \), drain resistance \( R_d \), channel resistance \( R_{ch} \), barrier height \( \phi_b \), and the ideality factor \( n \) were measured before and after accelerated stress tests. Typical data showing characteristic changes as a result of the DC bias life tests at 200°C and 110 hours are shown in Table 1 for the pHEMT.

Table 1: Parameter Changes Due to DC Bias Life Testing at 200° and 110 Hours

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Initial</th>
<th>After (200°C/110 hours)</th>
<th>D</th>
</tr>
</thead>
<tbody>
<tr>
<td>( R_s ) (ohm)</td>
<td>4.3</td>
<td>12.5</td>
<td>8.2</td>
</tr>
<tr>
<td>( R_d ) (ohm)</td>
<td>7.8</td>
<td>20.0</td>
<td>12.2</td>
</tr>
<tr>
<td>( R_{ch} ) (ohm)</td>
<td>19.5</td>
<td>22.7</td>
<td>3.2</td>
</tr>
<tr>
<td>( f_b ) (EV)</td>
<td>0.75</td>
<td>0.75</td>
<td>0.0</td>
</tr>
<tr>
<td>( h )</td>
<td>1.70</td>
<td>1.75</td>
<td>0.05</td>
</tr>
</tbody>
</table>

In the above case, the \( R_s \) and \( R_d \) changes may be attributed to ohmic contact interdiffusion, while the \( R_{ch} \) change may be dominated by traps in the channel.

**Experimental Results**

**Failure Distributions**

The failure distribution for the pHEMTS, assuming a lognormal distribution, is shown in Figure 2 for channel temperatures of 180°C, 195°C and 210°C. The straight line fit of the data indicates the validity of the lognormal distribution function and in the utilization of a single activation energy in explaining the results. A similar distribution plot was obtained for the single channel high electron mobility transistors (sHEMTs). The activation energy calculated from the data for the sHEMTs is 1.05eV. The extrapolated median time to failure at typical bias temperatures of 110°C is 10x10^4 hours for sHEMTs and 4x10^4 hours for double channel high electron mobility transistors (dcHEMTs). The reliability data indicates that the higher doping in the channel results in a shorter life for the dcHEMT.

**Failure Mode Analysis**

The pHEMT and sHEMTs were analyzed by DLTS techniques after accelerated life testing at 210°C. Besides the techniques based on capacitance and current DLTS, both the transistor transconductance and low frequency 1/f noise are considered as two parameters sensitive to deep levels, dislocations and interface states. Defects in both the dcHEMTs and sHEMTs are similar, as shown in Figure 3. Levels at 470 meV and 550 meV from the conduction band were detected and are similar to minority carrier traps due to dislocations present in HEMT layers where the InGaAs thickness exceeds the critical layer thickness. Since no minority carrier traps were present in the dcHEMTs or sHEMTs prior to accelerated life testing, we conclude that such traps in the InGaAs layer were generated as a result of the reliability tests.

continued on next page »»
In addition, the low frequency spectrum (1/f) shows a frequency dispersion in transconductance indicative of both interface and surface states. The \( g_m(f) \) characteristics at low frequencies indicate instabilities in the transistor which may be due to trapping at deep levels or interface states. Further, current DLTS measurements were performed on sHEMTs using relaxed geometry FET structures and, again, the spectrum shows only minority like traps indicative of dislocations and no presence of majority carrier traps. The structure of the FET had a channel thickness of 250Å, which is beyond the critical thickness, and is characterized by strain relief dislocations in the channel.

In order to attain a better correlation between the minority carrier traps and dislocations in the channel, dcHEMTs were analyzed by cross section TEM (XTEM) and planer TEM techniques. The InGaAs planer TEM image of the dcHEMT indicates the presence of edge dislocations in the cross sectional image. The planer TEM image indicates edge dislocation tips, propagating in a nearly perpendicular direction to both the [110] and [100] directions. The direction of climb is as expected for the zinc blend or diamond structure. The dislocation density after accelerated life testing has been measured to be in excess of \( 10^9 \text{ cm}^{-2} \), which represents a significant increase from \( 10^7 \text{ cm}^{-2} \) prior to testing. Figure 4 shows the morphology of dislocations generated at the substrate-epitaxial layer interface as well as dislocations generated at the InGaAs/GaAs interface.
Noise Parameters
The deep minority carrier traps in the InGaAs were further investigated by measuring the noise parameters: $T_{\text{min}}$, minimum noise temperature, $Z_{g,\text{opt}}$, optimum source impedance, and $g_m$, the noise conductance. The noise parameters were measured in a single-stage amplifier configuration at room temperature and up to 150°C. The source impedance measurement allows us to probe changes in both gate resistance and channel resistance introduced by accelerated stress testing where the source impedance is given by:

$$Z_{g,\text{opt}} = (R_g + R_{ch})_{\text{opt}} + jX_{g,\text{opt}}$$

The room temperature noise parameters of both the dcHEMT and sHEMT are shown in Table 2 after accelerated stress testing at 210°C for 100 hours. For comparison, the results of the sHEMT noise characteristics are also given. As shown in Table 2, an increase in the minimum noise temperature and $(R_g + R_{ch})$ occurred in both the dcHEMT and sHEMTs in comparison with a typical noise temperature of 82-90°C measured prior to reliability testing. The increases in $T_{\text{min}}$ observed further collaborates the observation that traps in the InGaAs channel introduce a hole emission/capture process which is still present at room temperature after reliability testing. The trapping phenomenon has also affected the dependence of the transconductance $g_m$ on drain current as shown in Table 2.

Table 2: Noise Parameters of dcHEMTS and sHEMTS Taken at Room Temperature Before and After Degradation

<table>
<thead>
<tr>
<th>$I_{ds}$ (mA)</th>
<th>$V_{ds}$ (V)</th>
<th>$T_{\text{min}}$ (°K)</th>
<th>$R_{g,ch}$ (opt) (Ω)</th>
<th>$X_{g,\text{opt}}$ (Ω)</th>
<th>$g_m$ (mS)</th>
</tr>
</thead>
<tbody>
<tr>
<td>sHEMT</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>210°C/100 hours</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>5</td>
<td>1.5</td>
<td>119</td>
<td>19.9</td>
<td>47</td>
<td>8.4</td>
</tr>
<tr>
<td>10</td>
<td>1.5</td>
<td>115</td>
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<td>46</td>
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<tr>
<td>15</td>
<td>1.5</td>
<td>111</td>
<td>23.0</td>
<td>45</td>
<td>6.2</td>
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<td>pHEMT</td>
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<tr>
<td>210°C/100 hours</td>
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<td></td>
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<td></td>
</tr>
<tr>
<td>5</td>
<td>2.5</td>
<td>124</td>
<td>26.0</td>
<td>40</td>
<td>10.3</td>
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<td>107</td>
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<td>38</td>
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<tr>
<td>sHEMT</td>
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<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Before</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>5</td>
<td>3.5</td>
<td>90</td>
<td>12.0</td>
<td>49</td>
<td>9.2</td>
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<td>3.0</td>
<td>83</td>
<td>13.2</td>
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<td>9.9</td>
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<tr>
<td>15</td>
<td>2.5</td>
<td>82</td>
<td>14.0</td>
<td>40</td>
<td>10.9</td>
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</table>

continued on next page >>
The space charge in the InGaAs layer, equal to the sum of the ionized donors and trapped charge, varies with $I_{ds}$, indicating stronger interaction between the two-dimensional electron gas (2DEG) and traps and screening of conduction electrons for higher current. These experiments show that the mechanism responsible for the changes observed during accelerated stress testing is related to the introduction of traps and is also a source of additional noise even at frequencies as high as 8.0 GHz. Trap occupancy, however, is determined among other factors by the bias conditions of the dcHEMT and sHEMT after cooling to room temperature. Both devices, however, exhibit dramatically different behavior upon illumination with light after reliability testing. The change in $V_{gs}$ voltage needed to sustain a drain current of 10 mA is large for the degraded dcHEMT (430 mV) and relatively small (6.5 mV) for the sHEMT. This observation points to different changes in both trap density and occupancy levels in both devices during accelerated testing and before illumination with light.

**Discussion of Results**

The growth on (100) GaAs buffer layers showed a high density of the crater defects (inverted triangular faceted pyramid) when viewed under the optical microscope. Lateral phase decomposition may also be evident in the InGaAs. The comparison of the above samples indicates no dependence on the mole fraction of aluminum, either in the GaAlAs (or InAlAs in the InP technology). These pyramid structures present faceted faces, forming inverted pyramids (Figure 4). The XTEM analysis allowed us to approximate the orientation of each facet. From other XTEM images, it is apparent that these inverted pyramids originated at the InGaAs/GaAs interface, and grew to the sample surface crossing both (InGaAs and GaAlAs) layers. The origin of these faceted defects was due to the growth inhibition of the InGaAs layer over the GaAs substrate. These samples also presented an important lateral contrast modulation, which was deduced from the XTEM observation. This contrast modulation was also initiated at the InGaAs/GaAs interface and then extended to the remainder of the layer, continuing to the GaAlAs upper layer. The lateral contrast modulation can be due to lateral decomposition or to a pure strain contrast. There is slight evidence of an ordered structure of CuPt-type. Due to the weakness of diffraction pattern maxima one cannot entirely conclude that the contrast is due to ordering. The XTEM data shows a quasi-periodic structure of contrast stripes perpendicular to growth axis of the GaAlAs and InGaAs layers. These images are summarized by the schematic of Figure 4. The presence of the defects does not depend on arsenic pressure, nor on growth temperature. The evidence of such defects presents the high degree of probability that the act as the defect centers for the trapping and detrapping phenomena observed as a result of the reliability testing.

**Summary**

The present investigation showed that pseudomorphic HEMTs degrade from traps in the InGaAs channel, probably due to the generation of dislocations in the strained, lattice mismatched layer. The minority carrier traps investigated by DLTS are identical to those created in layers which exceed the strain accommodation thickness 150 Å. The presence of dislocations in degraded pHEMTs was also clearly identified by TEM techniques. The degradation of noise characteristics and its relationship to channel traps has also been investigated. Finally, it has been shown that although doped channel pHEMTs have improved dc and rf performance, their reliability level is somewhat less compared to single channel conventional pHEMTs.

**Acknowledgements**

This investigation has been partially supported by the National Science Foundation as part of the Industry/University Cooperative Research Centers (IUCRC) program called Center for Optoelectronic Devices, Interconnects and Packaging (COEDIP).

**References**

Willie Mae Webb was born in Little Rock, Arkansas to Willie & Eula Webb. She received an associate degree from Bronx Community College in New York in Engineering Sciences and earned a BS degree in Electrical Engineering in May 1977 from Cornell University, where she also received the GE Minority Engineering Scholarship. From 1977-79 she worked for Honeywell Avionics in Minneapolis where, among other things, she established and reorganized the company’s Product Assurance Laboratory. From 1979 to 1980 she served in the USAF as a 1st Lieutenant and Bioenvironmental Engineer at Brooks AFB, Texas, and in the Air Force reserves after returning to Honeywell in 1980.

The desire for advancing knowledge was Miss Webb’s hallmark characteristic. She joined GE Aerospace Aircraft Electronics Division in Utica, New York in 1984, where her interest and experience in reliability engineering began. At GE, she worked as a reliability and quality assurance engineer. When she left GE in 1989, she entered the graduate program in Electrical Engineering at Syracuse University, earning her MS degree in August 1990. She later accepted a position with the Navy Air Warfare Center (NAVAIR) at Patuxent River, Maryland where she conducted research to determine critical real time display requirements of digital systems for the EA-6B aircraft.

Her proximity to the University of Maryland prompted her to pursue an MS degree in Reliability Engineering. She started this program in September 1991 and completed the degree requirements in 1993. Her immense interest in education and scholarship kept her at the University of Maryland, where she worked in advancing distance delivery of reliability engineering education. She worked in this capacity for the remainder of her career, during which she collaborated with nearly all of the professors in the program.

During her tenure at the University, her contribution and promotion of the reliability engineering program was substantial. One of her major scholarly contributions during her employment at the University of Maryland was the development of a two-volume book on “Applied Reliability Engineering”, which was co-authored with Professor Marvin Roush. This book has been used by numerous universities, organizations and individuals, and as the textbook for two senior-level reliability engineering courses at the University of Maryland. The RIAC has recently published this book as one of its products, with much success. She was near completion of another book on Probability Distribution Functions and Tables Used in Reliability Engineering. Unfortunately, her untimely passing did not allow her to complete this book. University of Maryland professors Mohammad Modarres and Ali Mosleh have graciously accepted the task of completing the book on Miss Webb’s behalf.

Besides being immensely modest and private, Miss Webb was also exceptionally generous, as exemplified by her donations to establish the Willie Webb Fellowship in Reliability Engineering at the University of Maryland. To honor her accomplishments and contributions to the field of Reliability Engineering, the University of Maryland Reliability Engineering Program has named its library the Willie Webb Reliability Engineering Library.
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| S M T W T F S | Sep 18, 2007 thru Sep 19, 2007 |
|  | Contact: American Society of Naval Engineers |
|  | Tidewater Section 0727 Avionics Loop, Bldg. LF18 USA |
| OCTOBER | RIAC Open Training Program // Las Vegas, NV USA |
| S M T W T F S | Sep 18, 2007 thru Sep 20, 2007 |
|  | Contact: Pat Smalley, Reliability Information Analysis Center // P 877.363.7422 or 315.351.4200 // F 315.351.4209 // psmalley@theRIAC.org |
| NOVEMBER | First Annual Maintenance & Reliability Symposium // Houston, TX USA |
|  | Contact: Ed Foster // P 281.530.8711 x 350 // F 703.610.9005 // edfoster@mundycos.com |
| DECEMBER | 15th Annual SMRP Conference // Louisville, KY USA |
|  | Contact: SMRP Headquarters // P 800.950.7354 // F 703.610.9005 // smrp@sba.com |
| JANUARY 2008 | 11th Annual Systems Engineering Conference // San Diego, CA USA |
|  | Contact: Britt Bommelje, Associate Director // P 703.247.2587 // bbommelje@ndia.org |
|  | 2nd System Safety 2007 International Conference // London, UK |
|  | Contact: Institution of Eng & Technology // P +44 (0) 1438 765650 // F +44 (0) 1438 765659 // jacquie.lee@theiet.org |
|  | Zero Downtime 2007 // Scottsdale, AZ USA |
|  | Contact: Nick Depperschmidt, Equipment Protection Magazine |
|  | P 800.803.9488 x111 // nickd@infowebcom.com |
|  | DoD Maintenance Symposium & Exhibition // Orlando, FL USA |
|  | Contact: Nancy Eiben ,SAE International // P 724.772.8525 // naneiben@sae.org |
|  | RIAC Open Training Program // Orlando, FL USA |
|  | Contact: Pat Smalley, Reliability Information Analysis Center // P 877.363.7422 or 315.351.4200 // F 315.351.4209 // psmalley@theRIAC.org |
|  | 54th Annual Reliability and Maintainability Symposium (RAMS 2008) // Las Vegas, NV USA |
|  | Contact: www.rams.org |
|  | F 315.351.4209 // psmalley@theRIAC.org |
This Microsoft Excel Workbook is intended solely for users of the Reliability Information Analysis Center (RIAC) “Handbook of 217Plus™ Reliability Prediction Models” who do not currently use the RIAC 217Plus™ software program. It automates the grading and scoring of those questions related to the seven 217Plus™ system level model process factors (Parts, Design, Manufacturing, System Management, Induced, No Defect and Wearout), plus the Reliability Growth process factor. As such, the user should be familiar with the manual process of creating a system reliability prediction using the 217Plus™ methodology prior to using this spreadsheet.

The “Min Req’d Questions” tab represents the minimum set of questions that must be answered in order to produce a valid Process Grade PI-Factor for each of the failure cause areas. This tab reflects the same minimum number of questions that are programmed into the 217Plus™ software tool. The results of this minimum analysis are presented at the bottom of this tab.

If the user chooses to answer additional questions based on detailed knowledge of their organization’s processes, he/she can subsequently answer those questions on the remaining tabs of the Workbook (the answers already provided on the “Min Req’d Questions” tab are automatically linked into the other tabs). The results of this complete Process Grade Factor analysis are presented on the “FULL RESULTS” tab.

Discussion related to process grade scoring and weighting is provided in Sections 2.4.1 and 2.4.2 of the 217Plus™ Handbook. Appendix A of the 217Plus™ Handbook contains additional detail on the calculation of environmental screening strength as implemented within the 217Plus™ methodology, which is also represented by a tab in this Workbook.

The purpose of this Microsoft Excel Workbook is to estimate the net total life cycle cost (TLCC) impact of performing root cause failure analysis and corrective action (CA) identification, implementation and verification to improve system, product, assembly, component, part or process reliability. It is intended to be an aid to the decision-making process that can be used to justify (or not) the upfront financial investment needed to perform root cause failure analysis and CA for specific failure incidents and compare them to the savings that may be achieved over the long term by virtue of the improved reliability of the system, product, assembly, component, part or process. It should be noted that net TLCC impact may be only one factor in determining whether root cause failure analysis and CA should be pursued. Other factors that should be considered may include, but not be limited to, (1) the criticality of the item function, (2) safety/liability impacts associated with a failure (regardless of net TLCC), (3) contractual requirements, (4) schedule constraints and/or (5) resource constraints. Where cost is the sole determining factor, however, the results generated by this tool can be used to convince the user, his/her management, a Program Manager and Senior Management of the long-term financial benefits to the company of determining the root cause of a failure, and implementing the corrective action necessary to improve reliability.

The contents of this Workbook cover three separate areas for which root cause failure analysis and CA activities can be implemented. These areas are (1) Hardware, (2) Process and (3) Software. When doing the net TLCC calculations, the user fills in the relevant information in each of these three areas, as necessary, to adequately describe all of the actions needed to implement the full root cause analysis and CA process. For example, a hardware failure may result in a root cause analysis and corrective action process that is traced back to a defective process, or a need to change software. Therefore, the net TLCC analysis should include the various cost elements associated with each of these areas. The Hardware, Process and Software areas are subdivided into the following tabs: (1) the costs associated with performing root cause analysis (RCA Yes), (2) the costs associated with not performing RCA (RCA No), and (3) the net TLCC impact associated with that area (RCA Net TLCC). There is a summary tab (NET TLCC – SUMMARY) that combines the results to present the composite net TLCC impact that should be used to support the decision to proceed with root cause failure analysis and CA (or not) for that specific failure incident.
During the time period of 1996 - 2006 a great deal of progress has been made in the advancement of basic GaAs integrated circuit manufacturing technology. A well defined technology for manufacturing integrated circuits with a variety of different device profiles within the circuit, and with the provision for two level metallization for passive element formation and interconnections has been established. An understanding of the reliability issues has also taken place. Optical interconnects for optoelectronic integrated circuits have reliability problems similar to MMICs. The purpose of this book is to (1) address the issues affecting the reliability and the manufacture of GaAs MMICs and (2) present the industrial status (through an industrial data base) in addressing such issues as yield, throughput, design rules, chip architecture, reliability, design for yield and manufacturability, substrate qualification, choice of processing technology and current status of process related models and sensitivity analysis. The analysis and discussion of reliability problems for optical interconnects is also presented.
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