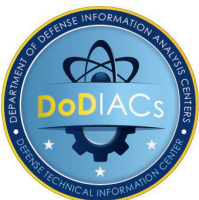


A Basic Introduction for Designing a PCB with EAGLE eCAD/CAM Software

October 28, 2020

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SURVICE Engineering Company
CCDC Army Research Laboratory



DSIAC is a DoD Information Analysis Center (IAC) sponsored by the Defense Technical Information Center (DTIC), with policy oversight provided by the Office of the Under Secretary of Defense (OUSD) for Research and Engineering (R&E). DSIAC is operated by the SURVICE Engineering Company.



Agenda

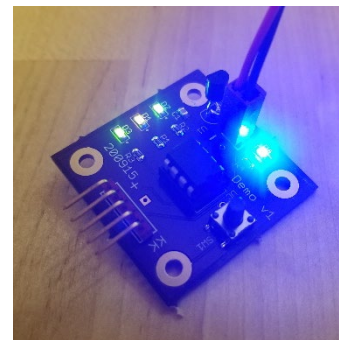
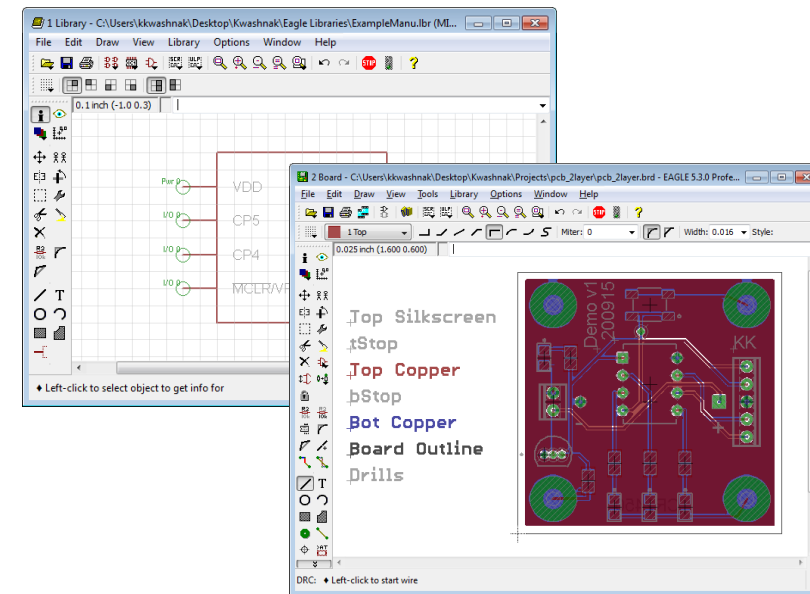
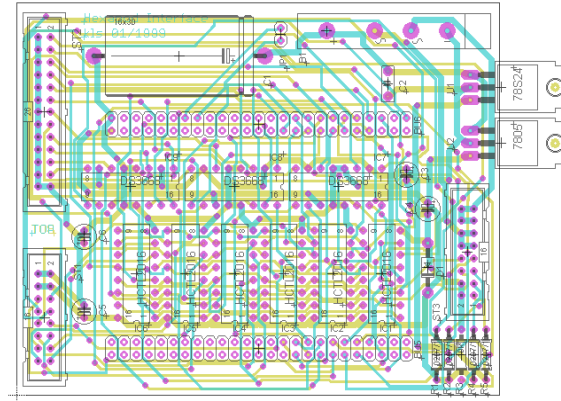
- Introduction

- Setup

- Creating a Component (Device)

- Two-Layer PCB Design

- Discussion



Agenda

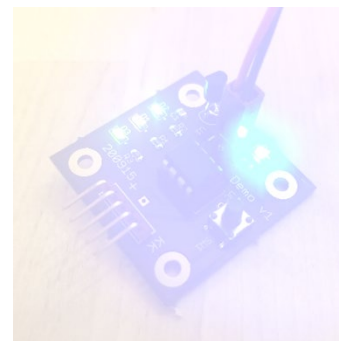
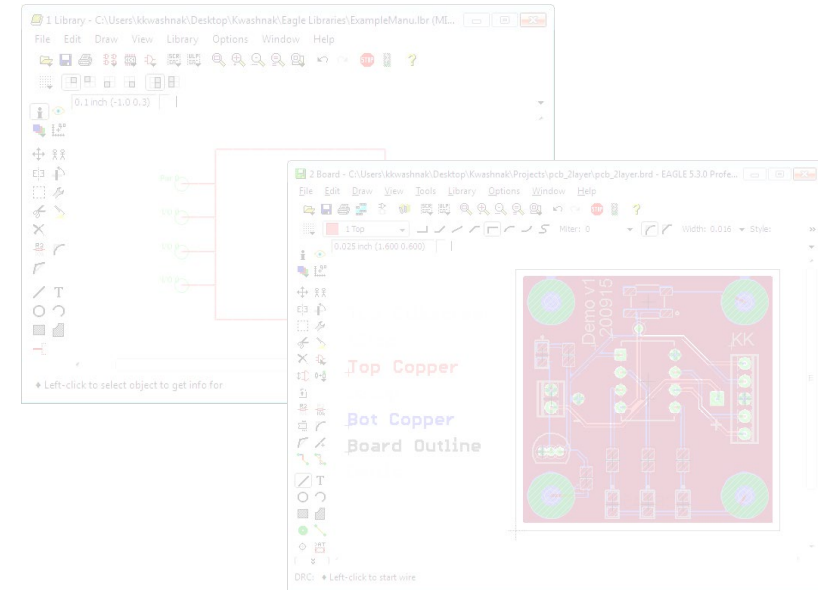
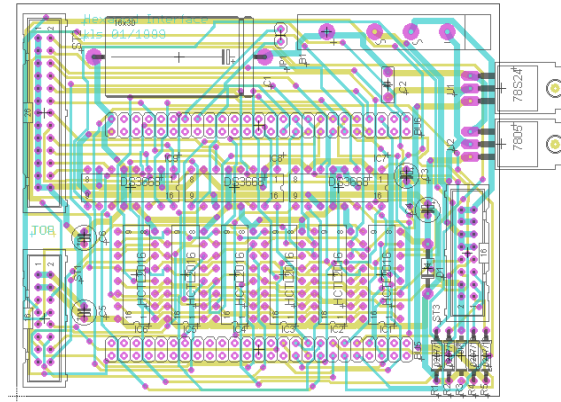
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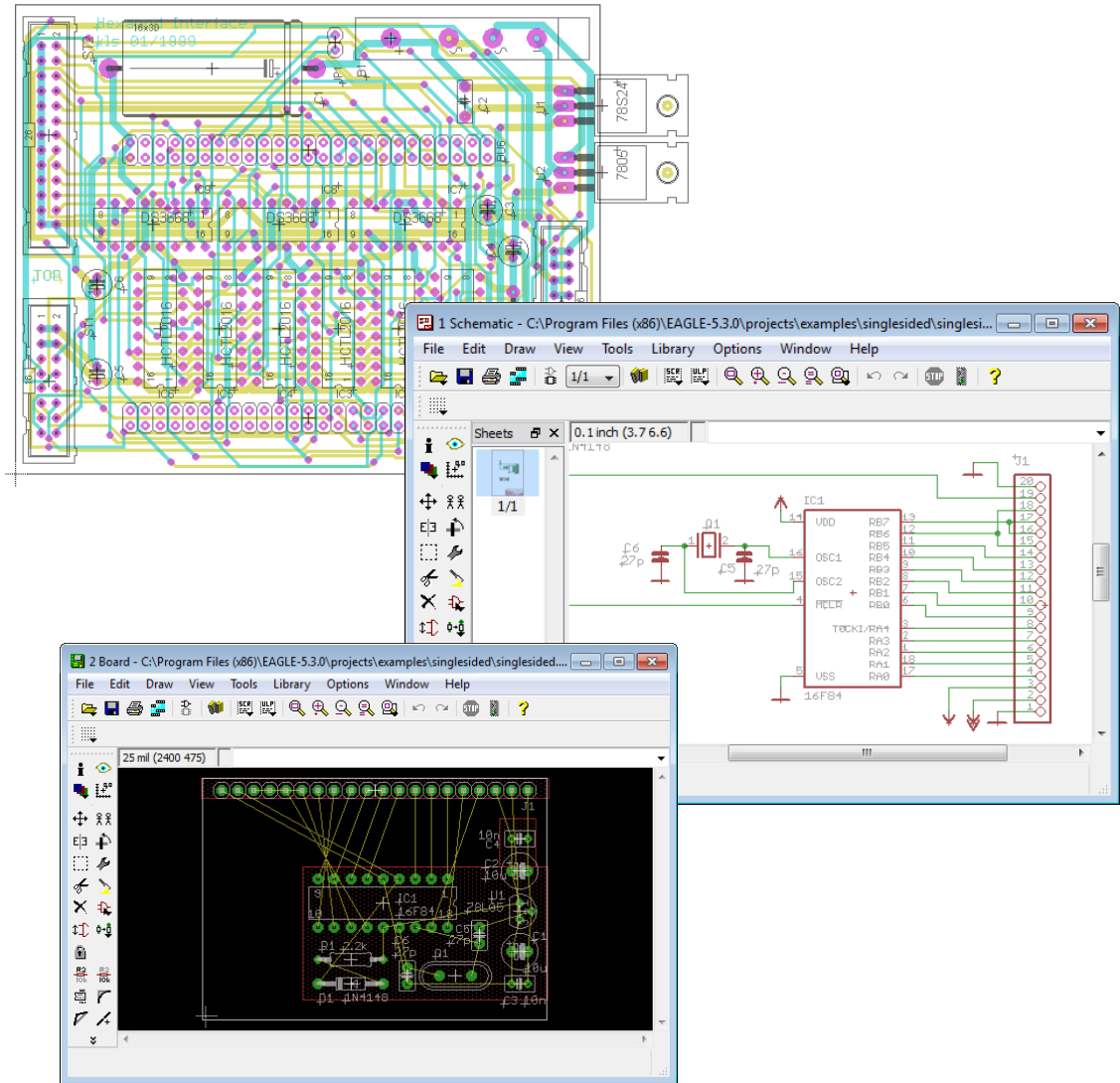
- Discussion



Introduction - Overview

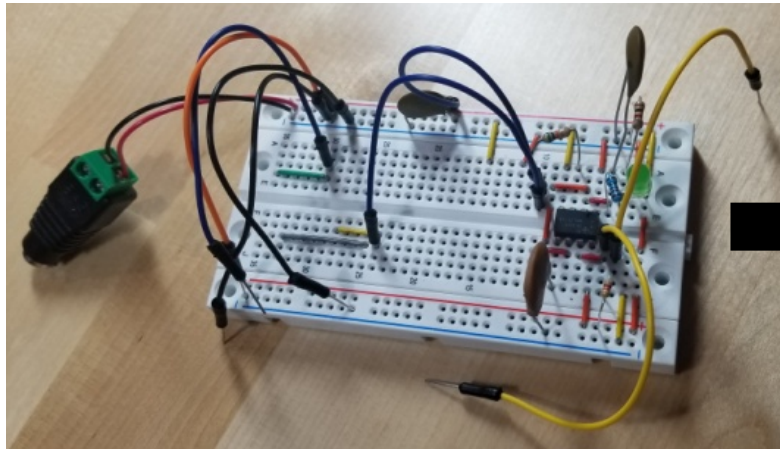
The Easily Applicable Graphical Layout Editor (EAGLE) is an electrical computer-aided design (eCAD) and manufacturing (CAM) software. EAGLE supports the designer in transitioning prototype hardware to a more controlled precision design.

Printed circuit boards (PCBs) are electrical circuits etched on assorted laminates via conducting material, such as copper, that branch through various layers of insulating dielectric to form interconnected networks.

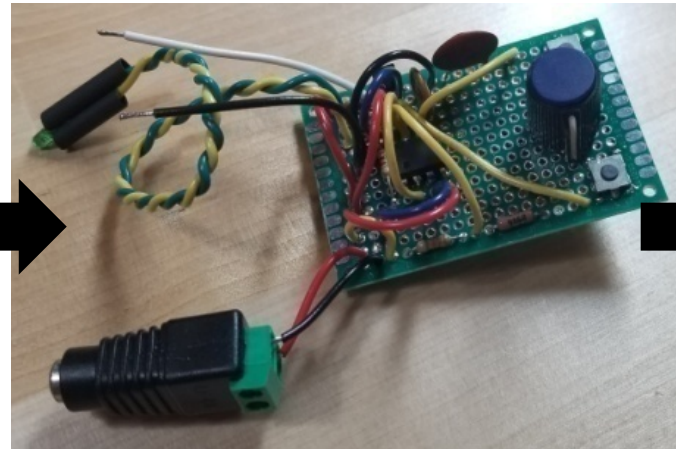


Introduction - Design Phases

Typical Phases of Transitioning From a Prototype to a Professional Design



Bread Board



Perf Board



PCB

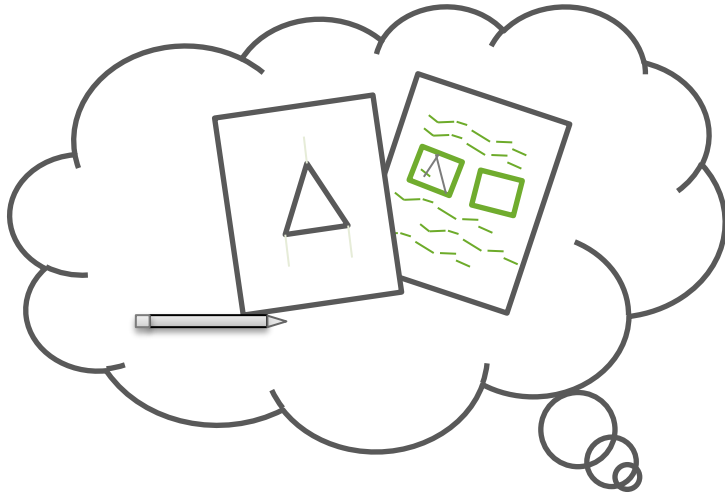
If the bread or perf board works, why make a PCB?

Quality. Assembly. Deterministic Behavior. Professional Look. Packaged. Requirements...

Introduction - eCAD

What do I need to create a PCB?

- All you will need is a pencil, paper, an idea, and a really clever manufacturer. However, that method will be costly, difficult to track, and time consuming.
- Not all manufacturers can guess what you need exactly, especially to conform to your requirements (they don't know what you don't write down, or they can guess and hope you like what they did).
- Essentially, you'll need an eCAD package that can captivate your idea and then generate the necessary manufacturing files. That's where the EAGLE eCAD software package comes into play.



Agenda

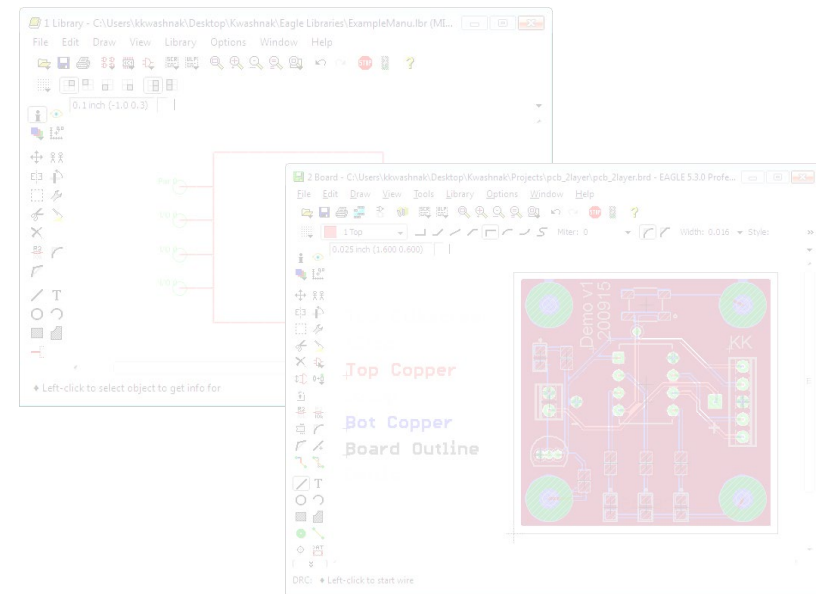
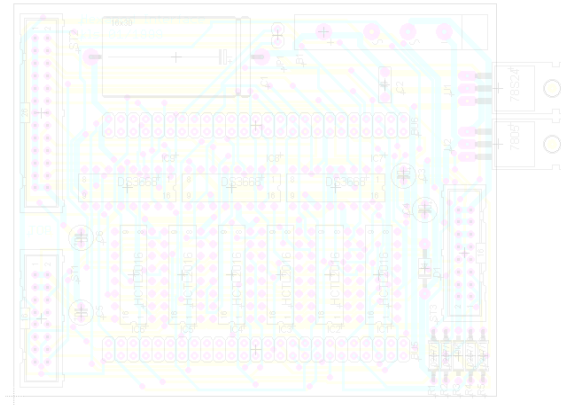
- Introduction

- Setup

- Creating a Component (Device)

- Two-Layer PCB Design

- Discussion



Setup - Circuit Programming and Testing

Line	Description	Manufacturer	PN	Q	Cost Per Item [\$]	Total [\$]
1	No Clean Solder Wire 0.031" Tin/Cpr Core 66. LF	Kester (1)	24-9574-7618	1	55.39 ¹	55.39
2	Soldering Station, 35W	Aoyue (2)	936	1	42.75 ²	42.75
3	No Clean Flux Paste Rosin	MG Chemicals (3)	8341-10ML	1	16.28 ¹	16.28
4	DC Linear Power Supply, Regulated, 0-30V, 0-5A	Korad (4)	KD3005D	1	85.00 ³	85.00
5	Banana to Clip Cable (Red and Black Wires)	B&K Precision (5)	TL 5A	1	10.10 ¹	10.10
6	Multimeter, True RMS	Fluke (6)	117	1	219.99 ¹	219.99
7	Desolder Braid No Clean, Rosin, Non Activated, LF	Chemtronics (7)	60-5-5	1	6.55 ¹	6.55
8	Assorted Hook-Up Wire	Sparkfun (8)	PRT-11375	1	16.95 ¹	16.95
9	Cable Stripper and Cutter, 20 ~ 30 AWG	Hakko (9)	CSP-30-1	1	14.06 ¹	14.06
10	Tweezer Set	Wiha (10)	44593	1	207.96	207.96
11	Isopropyl, Cleaning Agent	MG Chemicals (11)	824-1L	1	16.75 ¹	16.75
12	Brush	MG Chemicals (12)	855-5	1	4.45 ¹	4.45
13	PICKit3	Microchip (13)	PG164130	1	25.00 ⁴	25.00
14	PICKit3 Programming Cable	Digilent (14)	240-035	1	3.99 ¹	3.99
15	ESD Caliper	Wiha (15)	41105	1	74.56 ¹	74.56

1 - Data from Digikey on October 8, 2020

2 - Data from Aoyue3d on October 8, 2020

3 - Data from SRA Soldering Equipment on October 8, 2020

4 - Data from Amazon on October 8, 2020



Setup - PCB Components

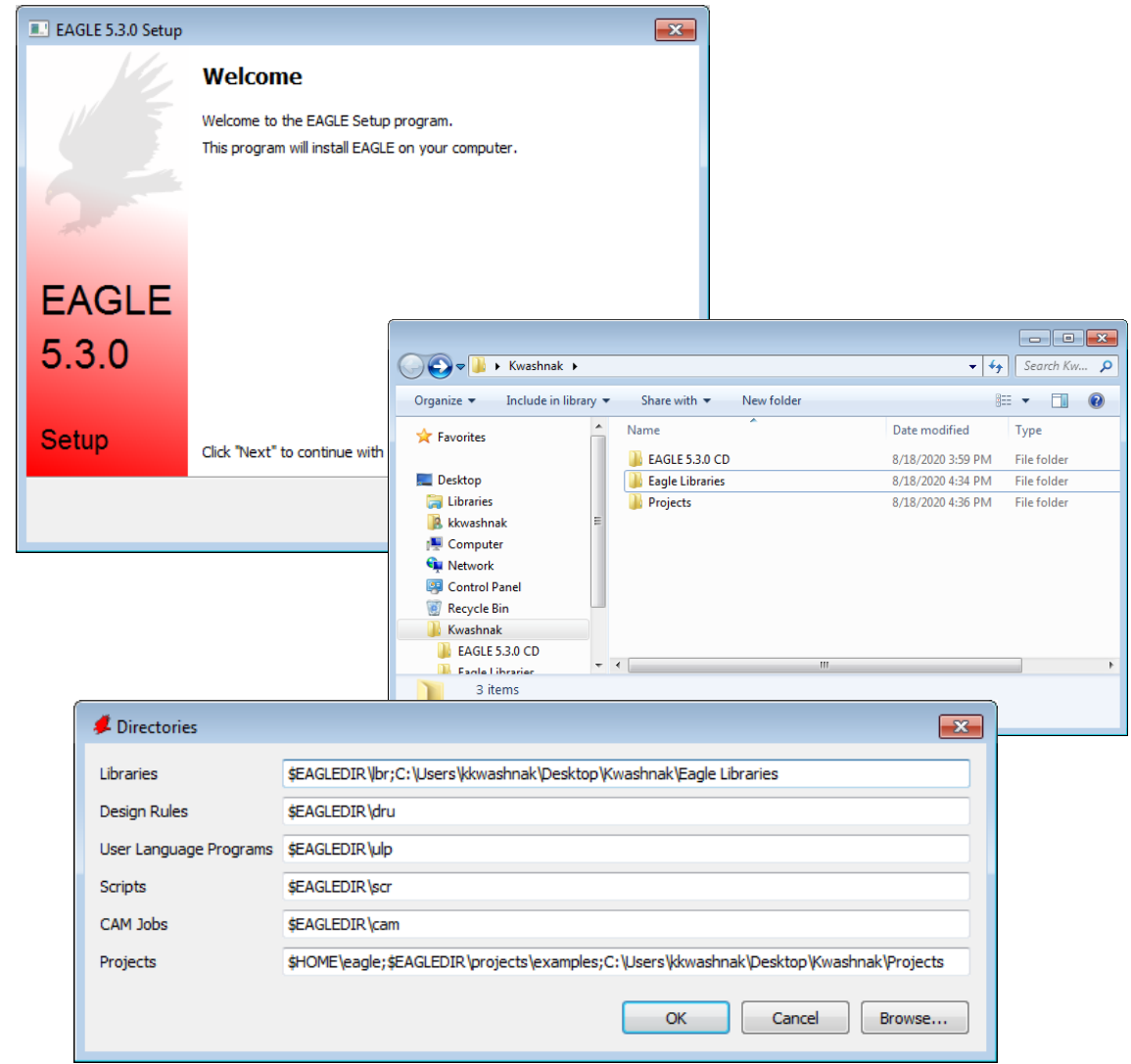
Line	Description	Manufacturer	PN	Q	Cost Per Item [\$] ¹	Total [\$]
1	Microcontroller, DIP8	Microchip (16)	PIC12LF1501	1	0.77000	0.77
2	IC DIP Socket 8POS	Adam Tech (17)	ICS-308-T	1	0.15000	0.15
3	Battery, CR2450, 3V	Energizer (18)	CR2450VP	1	1.19000	1.19
4	Battery Holder, Coin PC Pin	MPD (19)	BS-2450	1	1.09000	1.09
5	Regulator Linear 3V, TO92 -3	Microchip (20)	MCP1700-3002E/TO	1	0.37000	0.37
6	Green Smd LED	Dialight (21)	5988170107F	4	0.39000	1.56
7	Tactile Switch, NO	C&K (22)	PTS 647 SK38 SMTR2 LFS	1	0.13000	0.13
8	Res, 0805, 120?, 5%, 1/8W	Vishay Dale (23)	CRCW0805120RJNEA	4	0.10000	0.40
9	Cap, 0805, 0.1uF, 25V, X7R	KEMET (24)	C0805C104M3RACTU	1	0.10000	0.10
10	0.100" Header, 5 Pin, Prog	Molex (25)	22-23-2051	1	0.34000	0.34
11	0.100", Conn Housing, 5POS	Molex (26)	0022012057	1	0.23000	0.23
12	0.100" Header, 2 Pin, Batt	Molex (27)	22-23-2021	1	0.17000	0.17
13	0.100", Conn Housing, 2POS	Molex (28)	0022012027	1	0.11000	0.11
14	Conn 22-30AWG Crimp Tin	Molex (29)	0008650804	7	0.10000	0.70

1 - Price from Digikey as of September 18, 2020

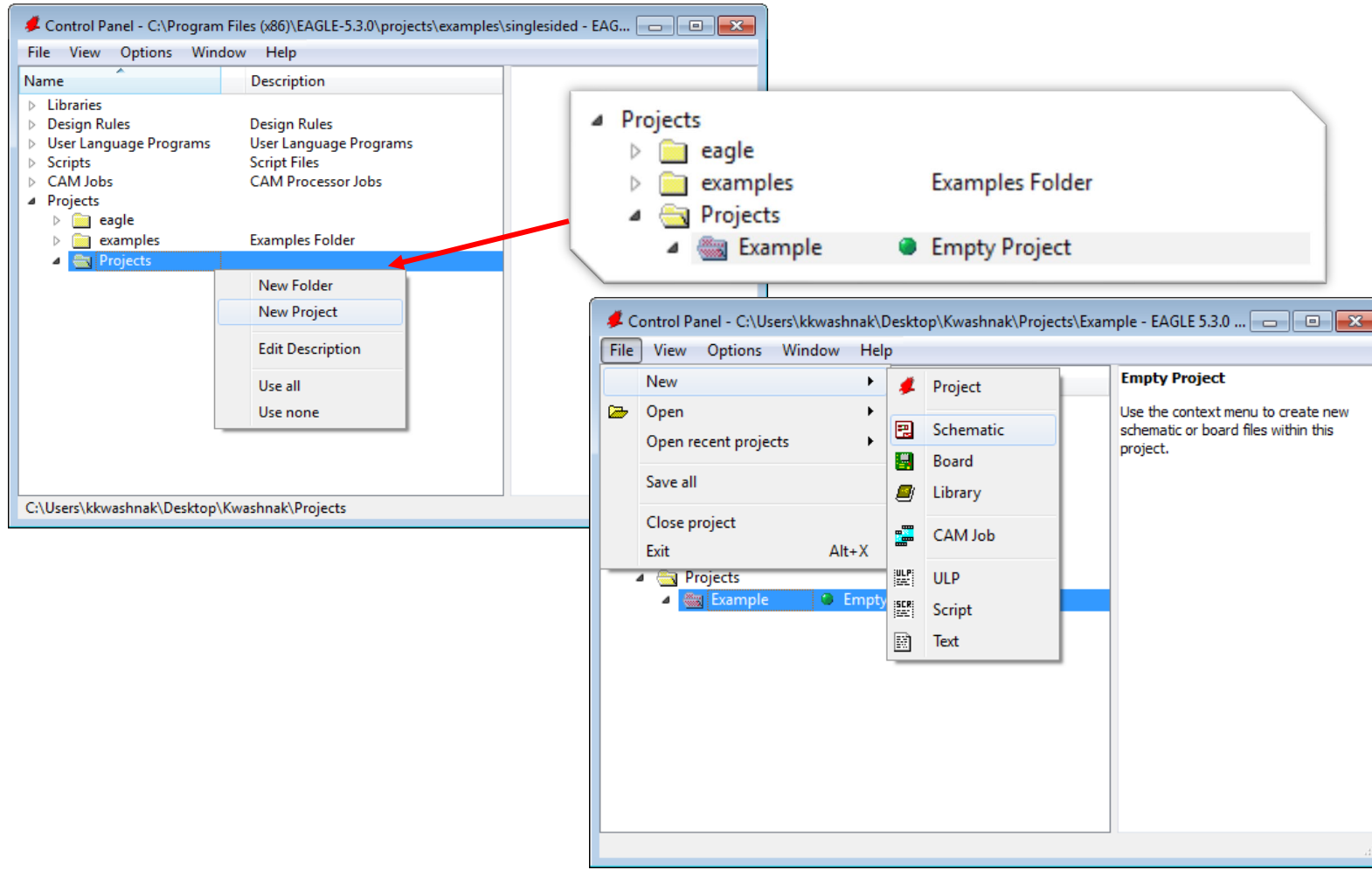


Setup - Computer

- Using a laptop with Ubuntu 16.04 OS, run an isolated Windows 7 x 64 virtual OS on VirtualBox v5.1.38
- Install software
 - EAGLE v5.3.0
 - MPLAB X IDE v5.4.0 and XC8 Compiler v2.30
- In virtual OS, form a file structure to house design records
- Add pathways to EAGLE's directories



Setup - Project



- Create a project
- Activate project
- Add file
 - Schematic
 - Board
 - Library
 - CAM job
 - ULP
 - Script
 - Text

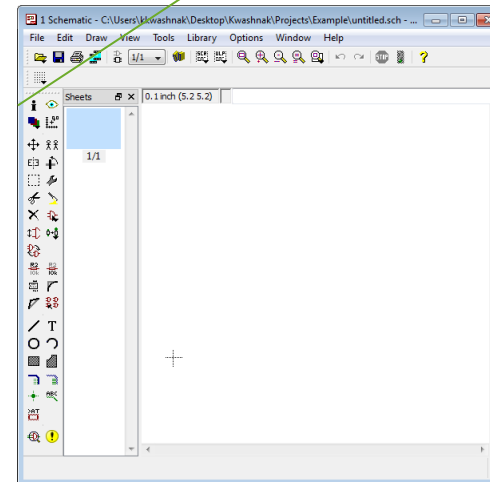
Setup - Software

Graphical Conventions

Schematic Editor					
#	Name	#	Color		Comment
1	Nets	91	Dark Green		
2	Buses	92	Dark Purple		Consists of multiple Nets
3	Pins	93	Dark Green		
4	Symbols	94	Dark Red		
5	Names	95	Dark Grey		
6	Values	96	Dark Grey		
7	Info	97	Dark Grey		
8	Guide	98	Dark Yellow		

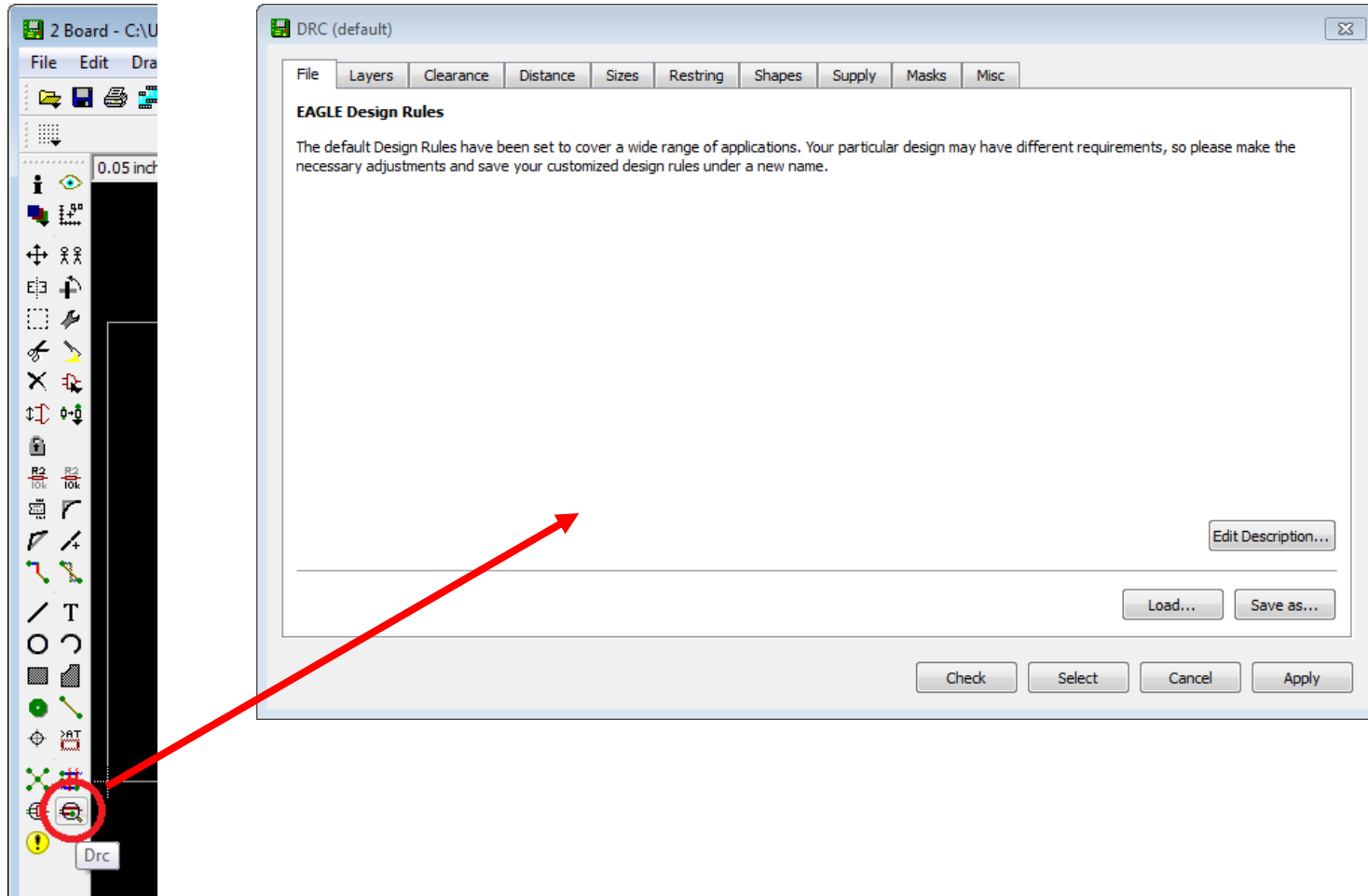
Board Editor								
#	Layer Group	Name	#	Color Name	Color		Comment	Gerber
1	Top Silkscreen	tPlace	21	Light Grey				.tslk
2	Green Top	tStop	29	Black with Line			Keep Out Region	.tstp
3	Top Copper	Top, Pads, Vias	1, 17, 18	Red, Dark Green, Dark Green				.tcpr
4	Bottom Copper	Bottom, Pads, Vias	16, 17, 18	Blue, Dark Green, Dark Green				.bcpr
5	Green Bottom	bStop	30	Black with Line				.bstp
6	Bottom Silkscreen	bPlace	22	Dark Grey				.bslk
7	Board Outline	Dimension	20	Light Green				.dout
8	Drills, Holes	Drills, Holes	44, 45	Dark Grey, Dark Grey				.ddrl
9	Top Restriction Zone	tRestrict	41	Red with Dots				
10	Bottom Restriction Zone	bRestrict	42	Blue with Dots				
11	Origins, Top	tOrigins	23	Light Purple			Part Manipulation	
12	Origins, Bottom	bOrigins	24	Dark Purple			Part Manipulation	
13	Name, Top Component	tNames	25	Light Grey			Appears on silkscreen	
14	Name, Bottom Component	bNames	26	Dark Grey			Appears on silkscreen	
15	Document Notes, Top	tDocu	51	Light Yellow			PCB Physical View	
16	Document Notes, Bottom	bDocu	52	Dark Yellow			PCB Physical View	

Toolbox

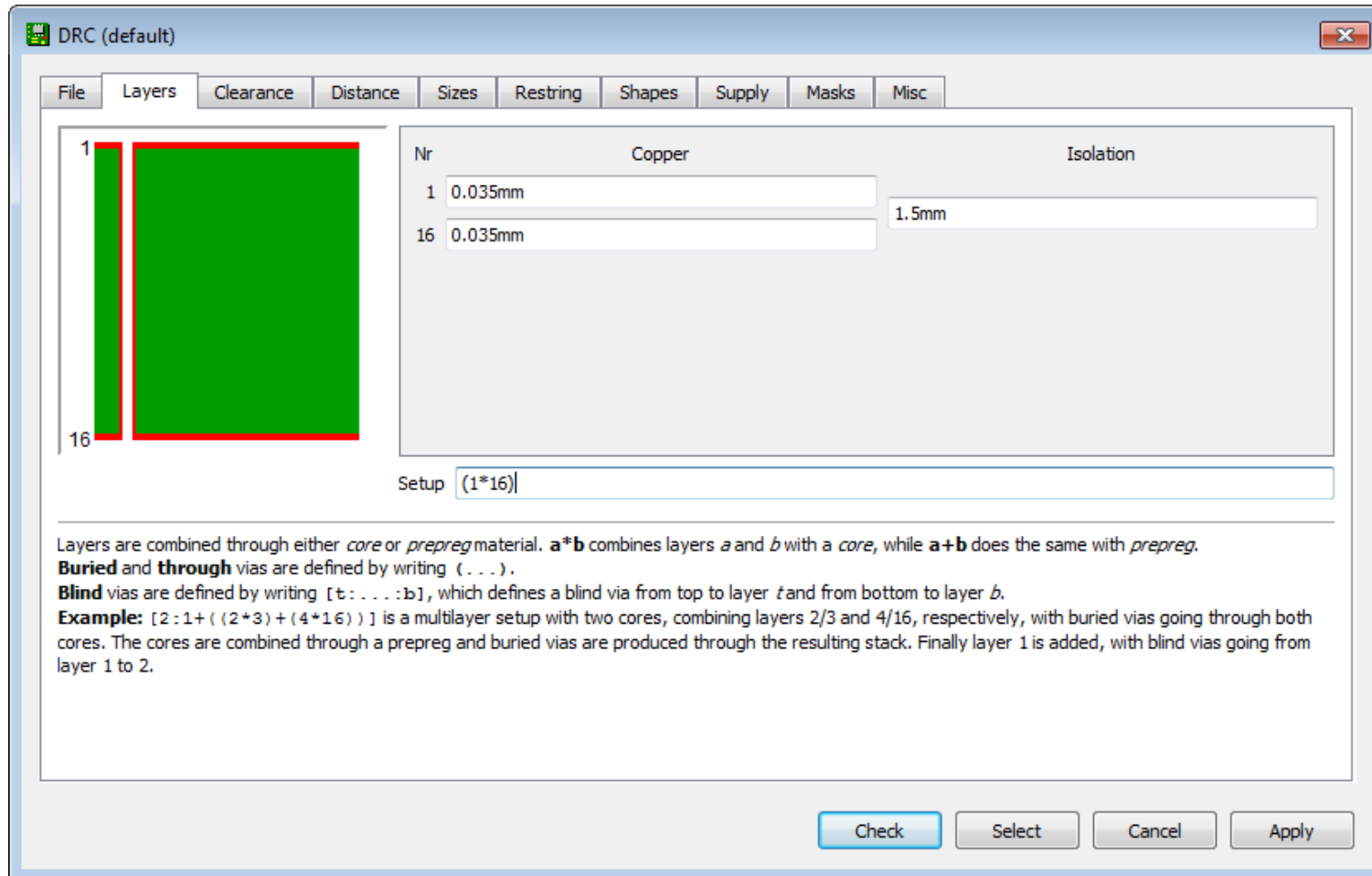


Setup - Design Manufacturing Requirements

- Toolbar button <Drc>
- Set requirements for board layout
 - Layers
 - Clearance
 - Distance
 - Sizes
 - Restring
 - Shapes
 - Supply
 - Masks
 - Misc.

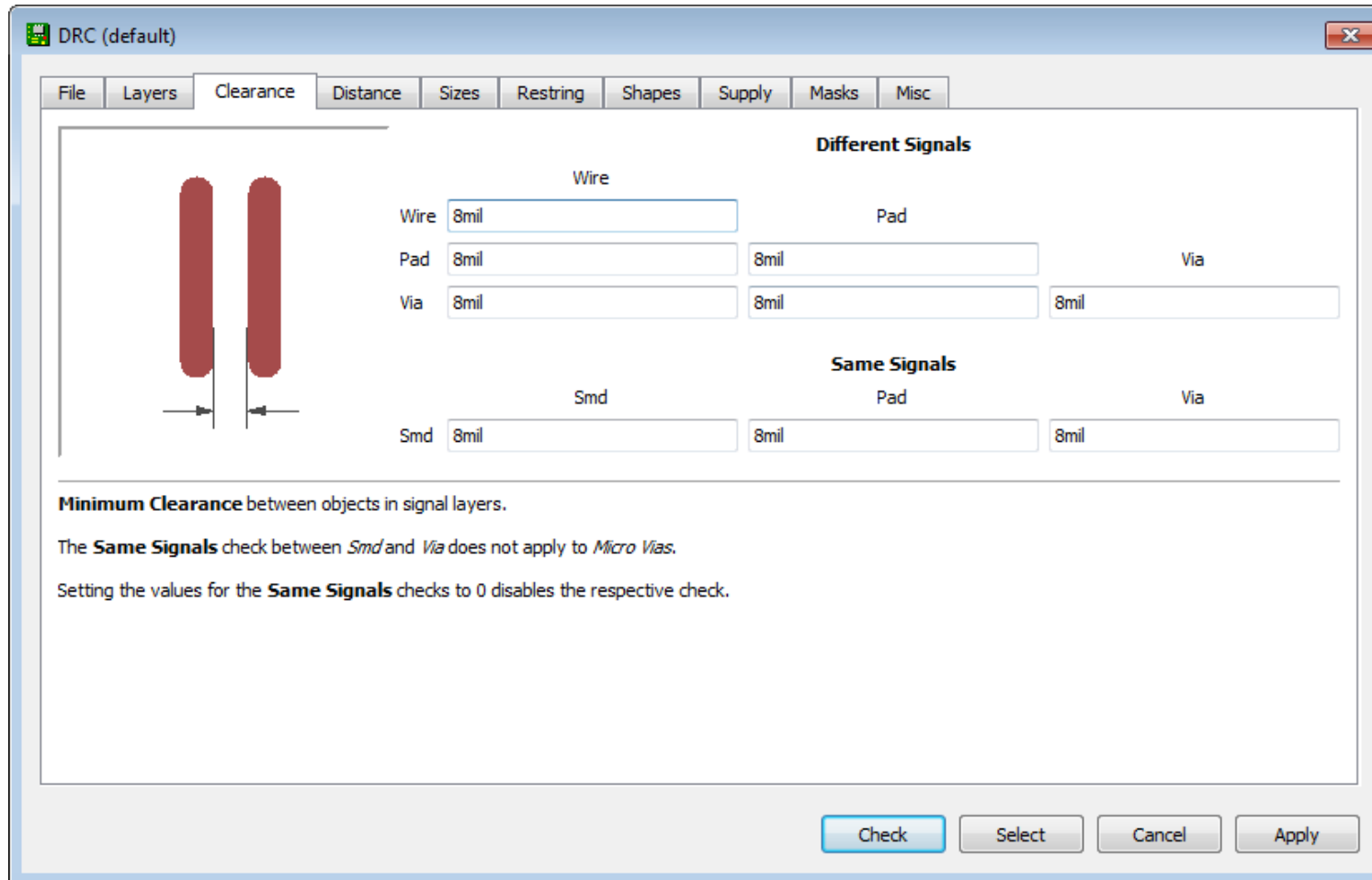


Setup - DRC, Layers



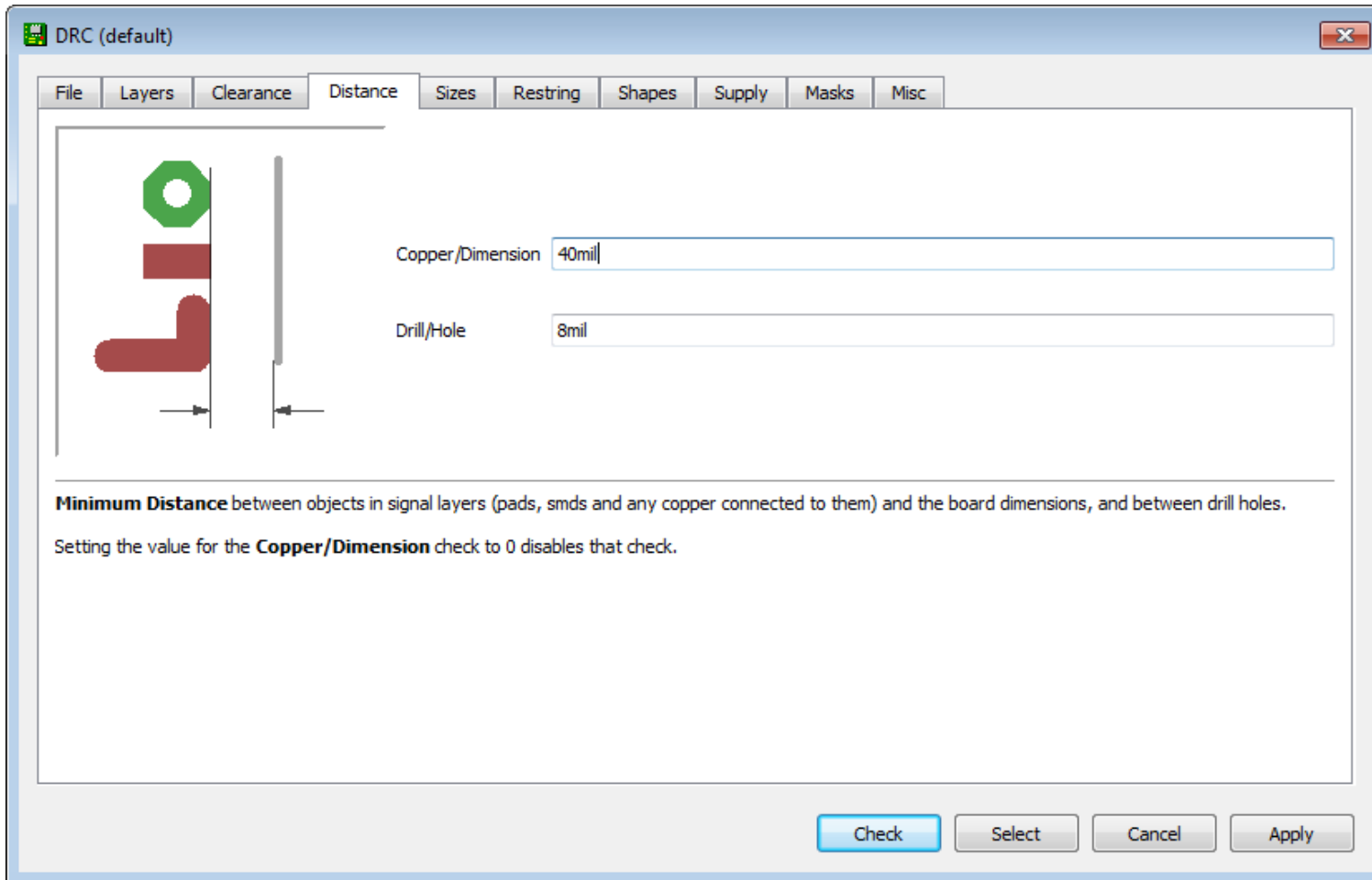
- Layer stack-up.
- The setup field defines the custom text field to define board stack-up.
- $(1*16) \Rightarrow$ two-layer board.
- $((1*2)+(15*16)) = ?$ multilayered board.
- $(2:1 + ((2*3)+(14*15))+15:16) \Rightarrow$ multilayered board with blind vias.

Setup - DRC, Clearance



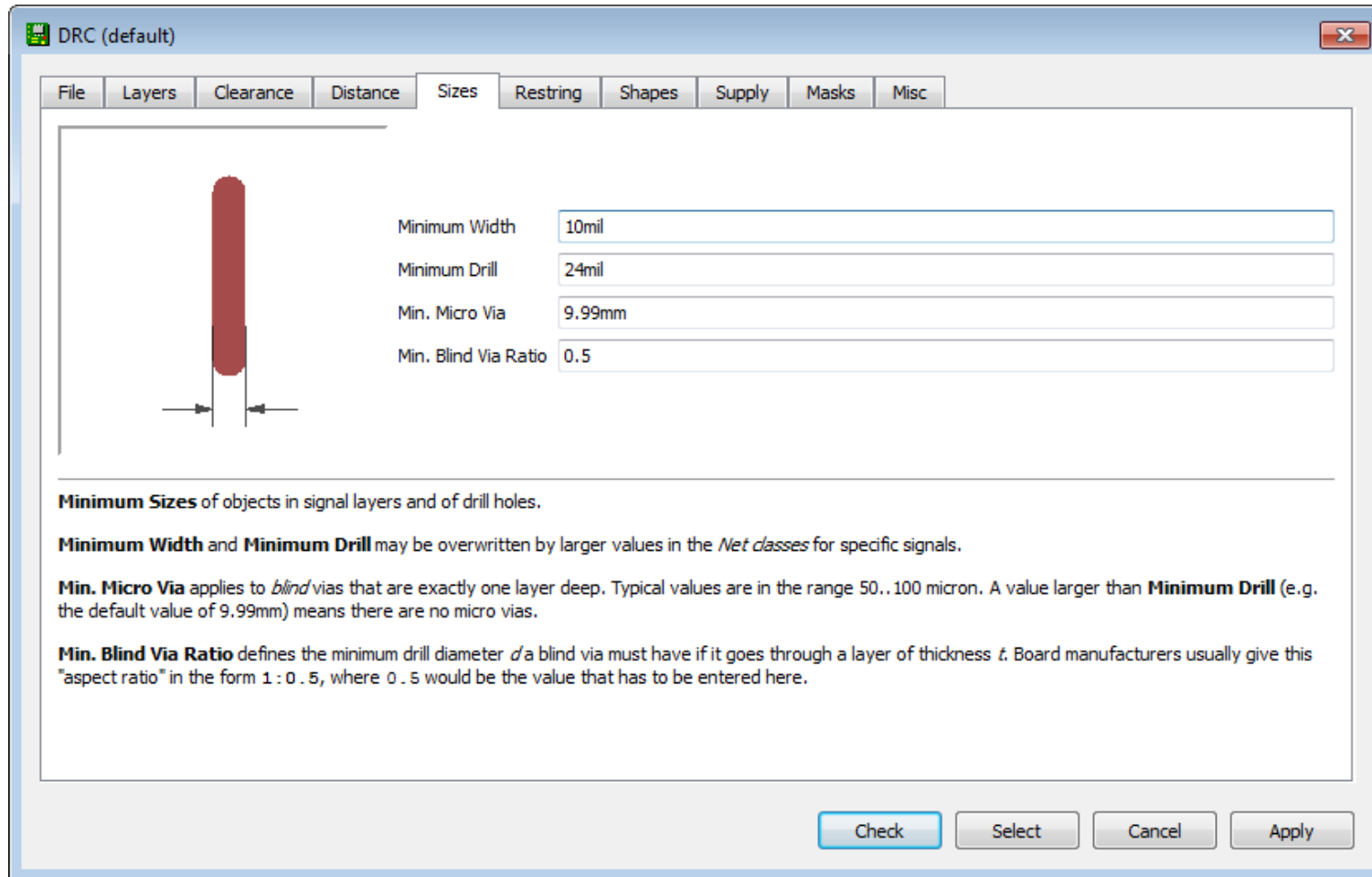
- Minimum distance between objects in signal layers
- Specify according to Wire, Pad, Via, or Smd

Setup - DRC, Distance



- Minimum distance between objects in signal layers, in addition to board dimensions and drill holes
- Specify according to copper or drill hole

Setup - DRC, Sizes



- Minimum width of any objects in the signal layers and drill holes

SETUP - DRC, Restring

	Min	%	Max	Diameter	
Pads	Top	10mil	25	20mil	
	Inner	10mil	25	20mil	<input type="checkbox"/>
	Bottom	10mil	25	20mil	
Vias	Outer	8mil	25	20mil	
	Inner	8mil	25	20mil	<input type="checkbox"/>
Micro Vias	Outer	4mil	25	20mil	
	Inner	4mil	25	20mil	

Restringing for pads and vias are defined in percent of the drill diameter (limited by **Min** and **Max**). If the diameter of an actual pad or via would result in a larger restringing, that value will be used in the outer layers.

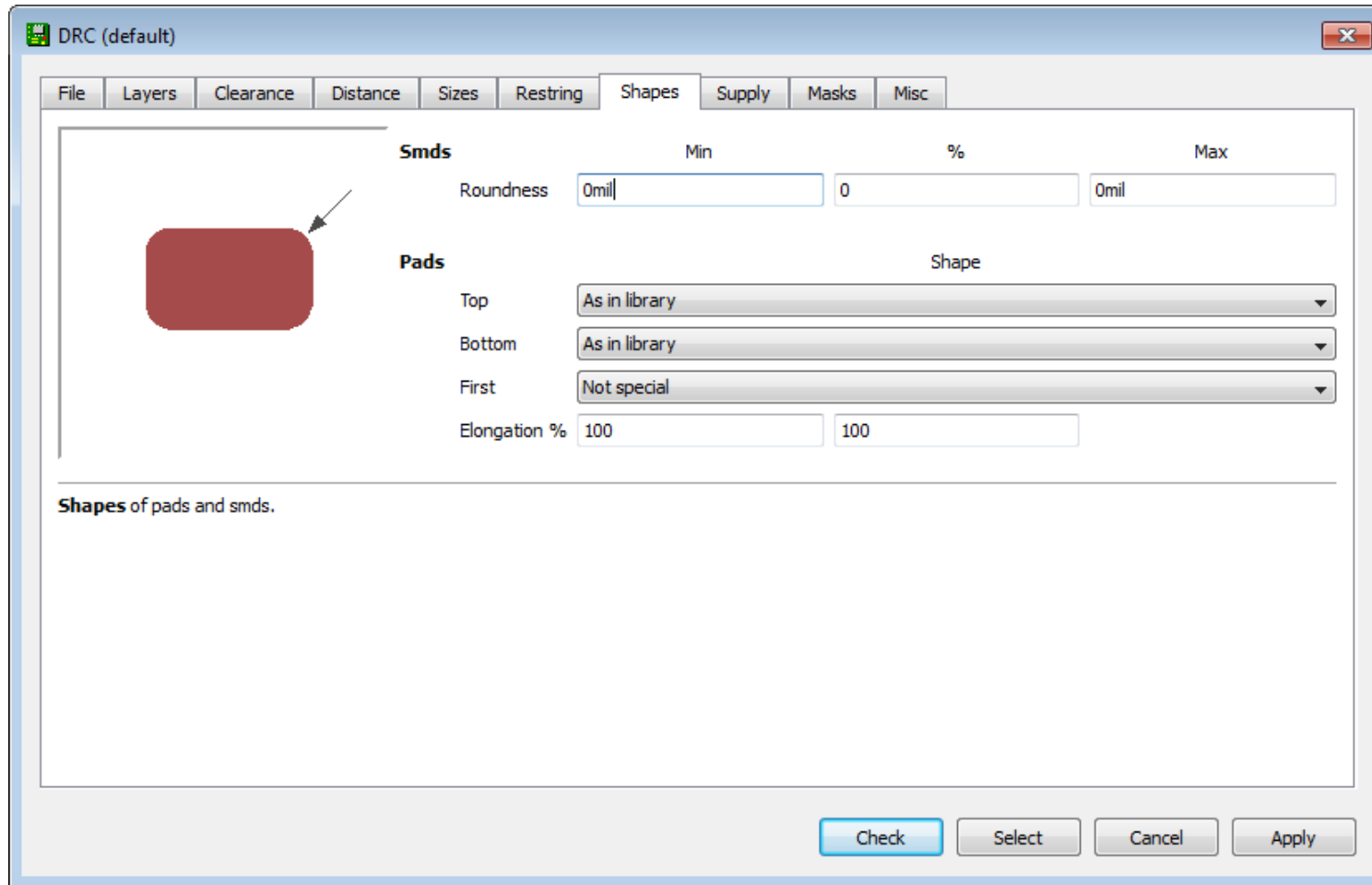
If the **Diameter** option is checked the actual pad or via diameter will be taken into account in the inner layers, too.

Micro Vias are *blind* vias that are exactly one layer deep and have a drill diameter that is smaller than the **Minimum Drill** value defined under *Sizes* (which may be overwritten by a larger **Drill** value in the *Net classes*).

Buttons: Check, Select, Cancel, Apply

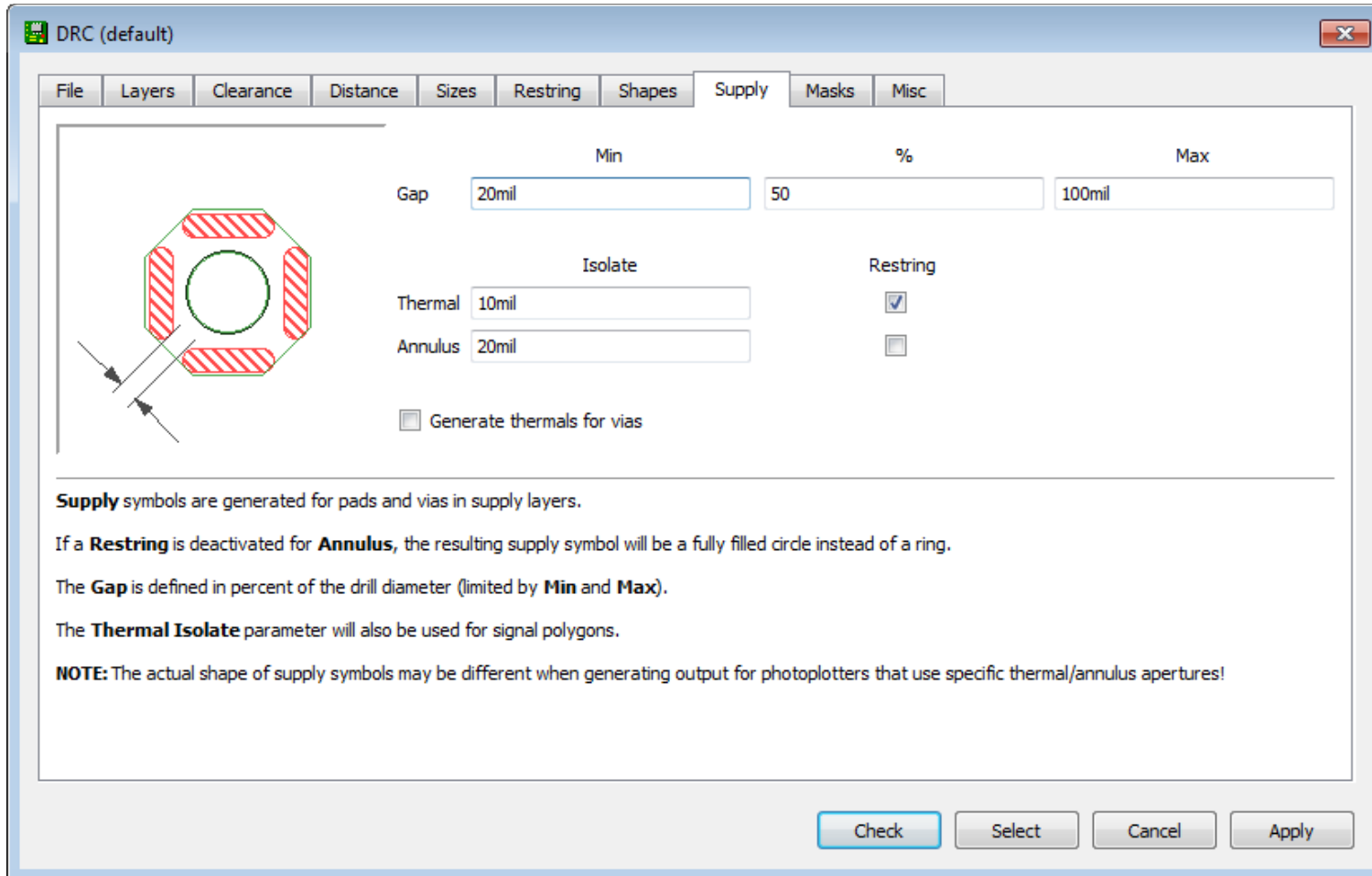
- Width of the copper ring that must remain after the Pad or Via has been drilled
- Specify per Pads, Vias, and Micro Vias

SETUP - DRC, Shapes



- Geometry of Pads and Smds

Setup - DRC, Masks



DRC (default)

File Layers Clearance Distance Sizes Restricting Shapes Supply Masks Misc

Gap Min % Max

Thermal Isolate

Annulus Restricting

Generate thermals for vias

Supply symbols are generated for pads and vias in supply layers.

If a **Restricting** is deactivated for **Annulus**, the resulting supply symbol will be a fully filled circle instead of a ring.

The **Gap** is defined in percent of the drill diameter (limited by **Min** and **Max**).

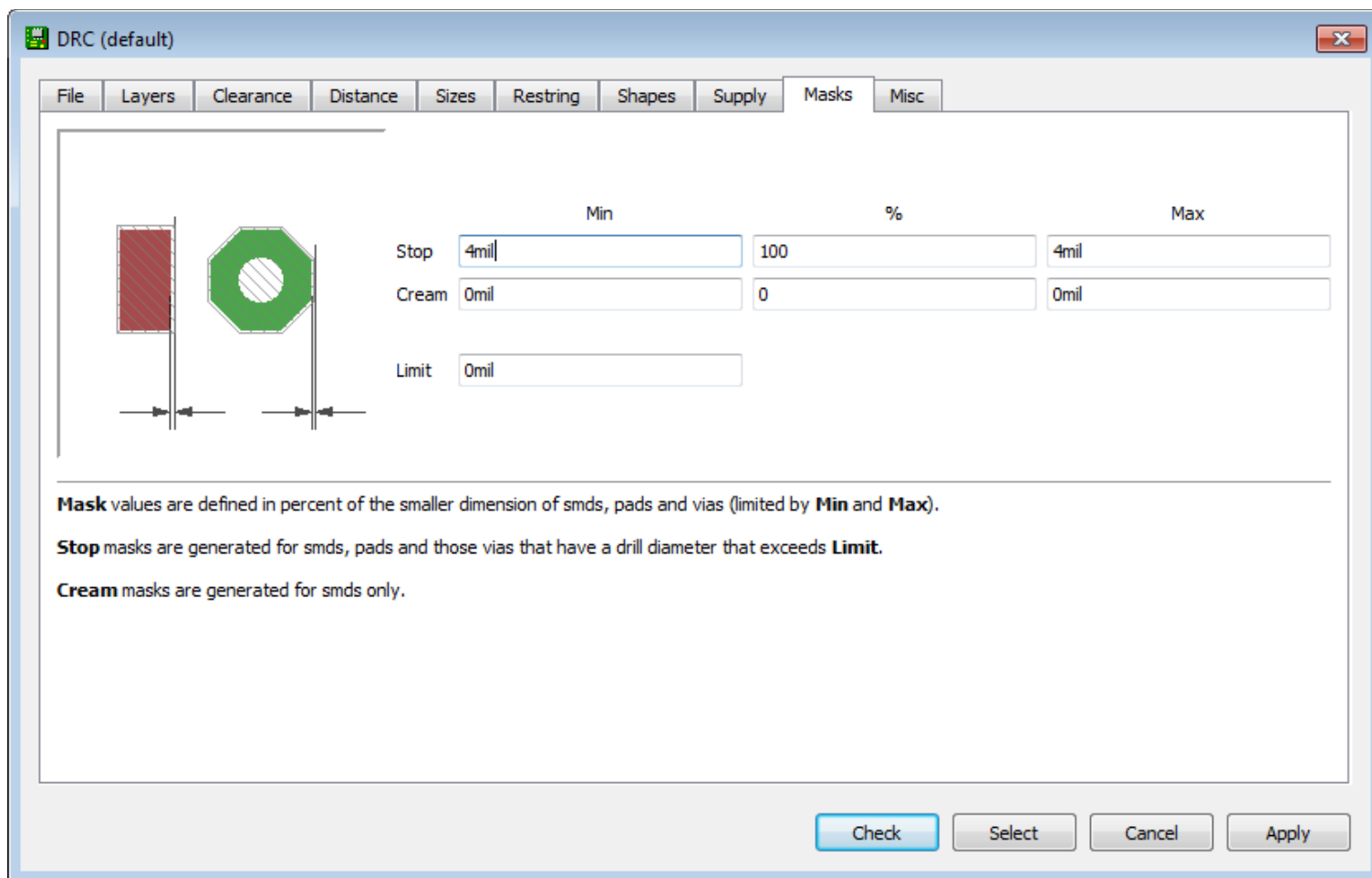
The **Thermal Isolate** parameter will also be used for signal polygons.

NOTE: The actual shape of supply symbols may be different when generating output for photoplotters that use specific thermal/annulus apertures!

Check Select Cancel Apply

- Geometry of the Thermal and Annulus symbols used in the supply layers

Setup - DRC, Masks (cont.)



	Min	%	Max
Stop	4mil	100	4mil
Cream	0mil	0	0mil
Limit	0mil		

Mask values are defined in percent of the smaller dimension of smds, pads and vias (limited by **Min** and **Max**).

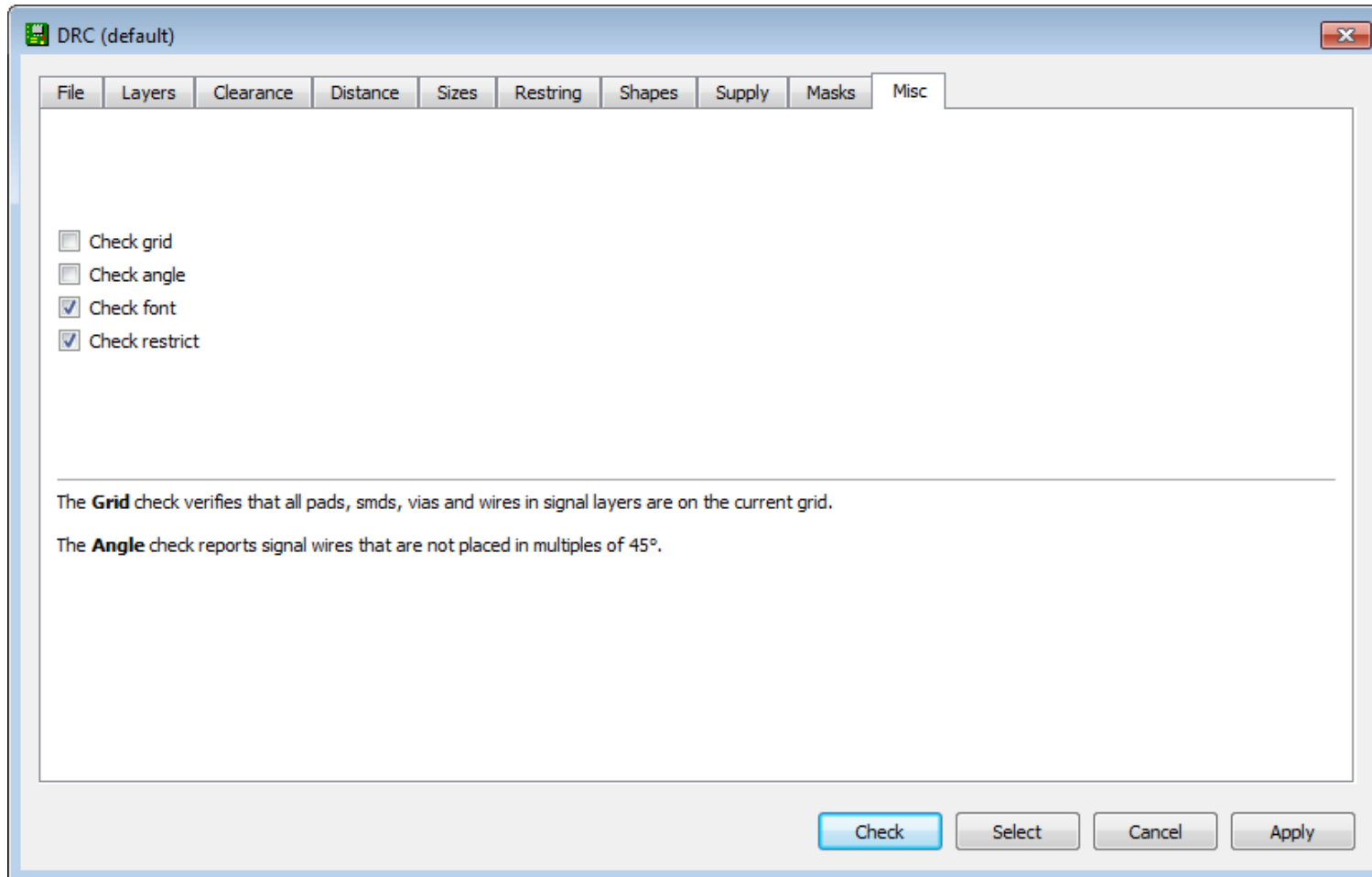
Stop masks are generated for smds, pads and those vias that have a drill diameter that exceeds **Limit**.

Cream masks are generated for smds only.

Buttons: Check, Select, Cancel, Apply

- Dimensions of the Solder Stop and Cream Masks

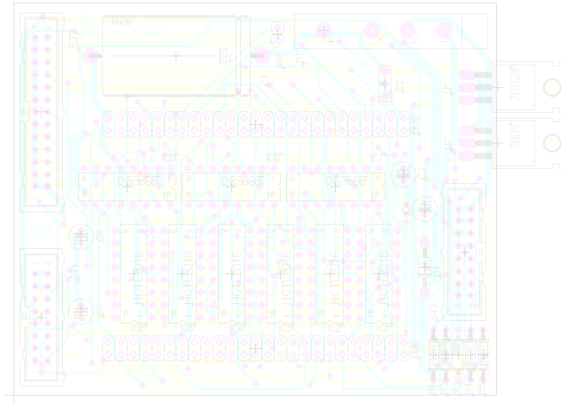
Setup - DRC, Miscellaneous



- Grid settings and Angle checks

Agenda

- Introduction

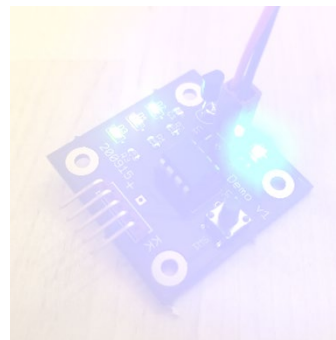


- Setup

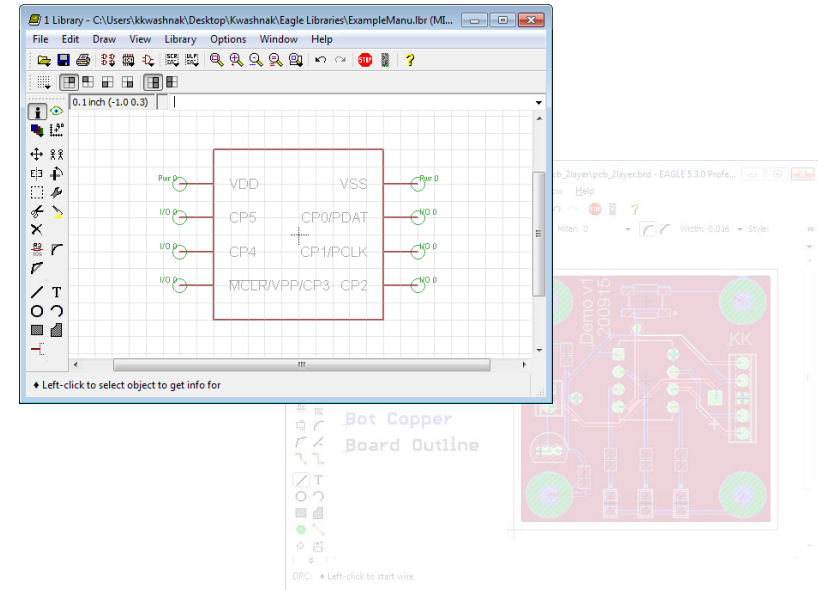


- Creating a Component (Device)

- Two-Layer PCB Design



- Discussion

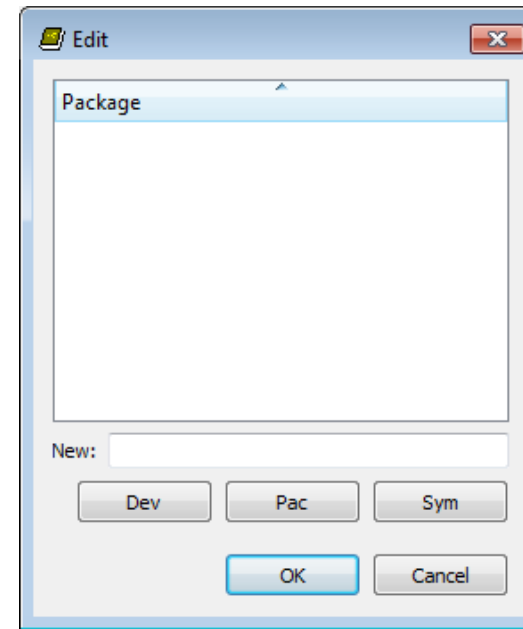
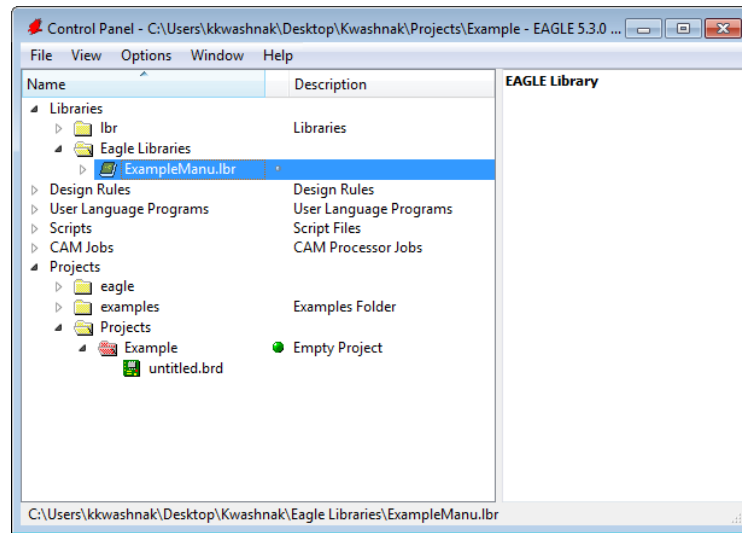


Creating a Component (Device) - Overview

A component comprises three main elements in EAGLE:

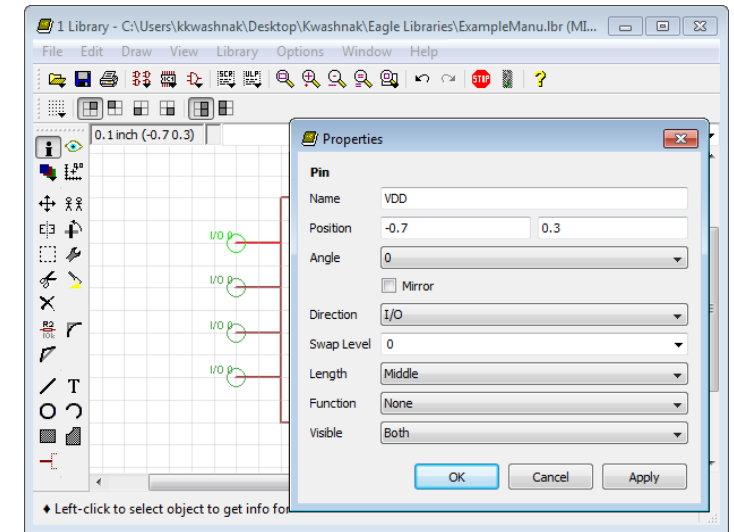
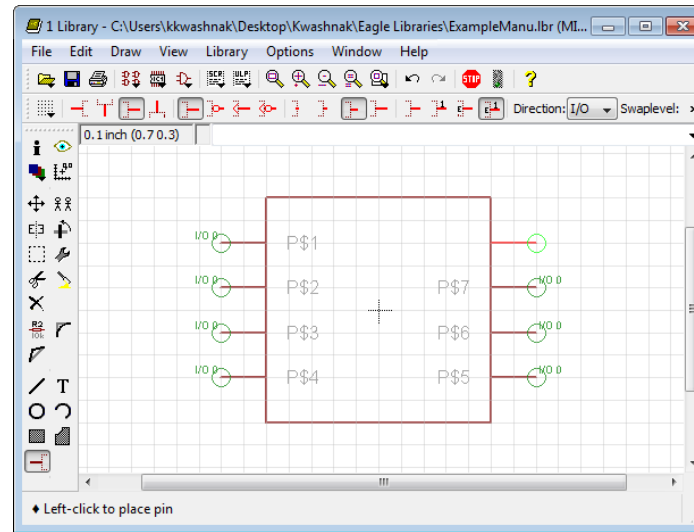
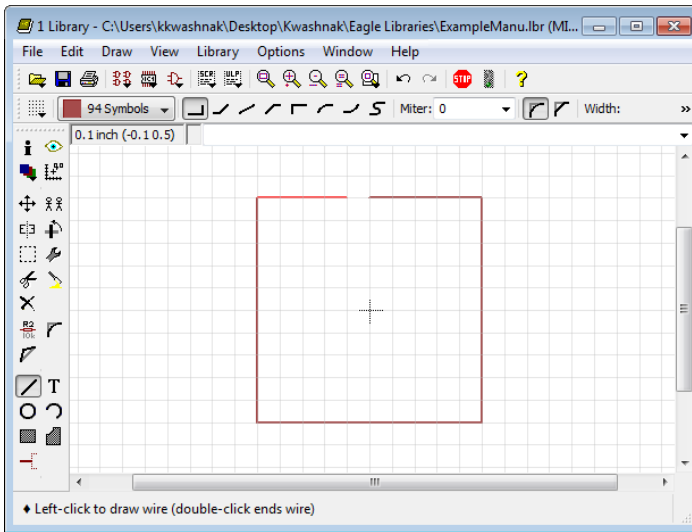
1. Symbol (used in the Schematic Editor)
2. Package (used in Board Editor)
3. Device (stored in library file that the Schematic and Board Editor reference)

The device is stored in a library, which houses various devices, symbols, and packages.



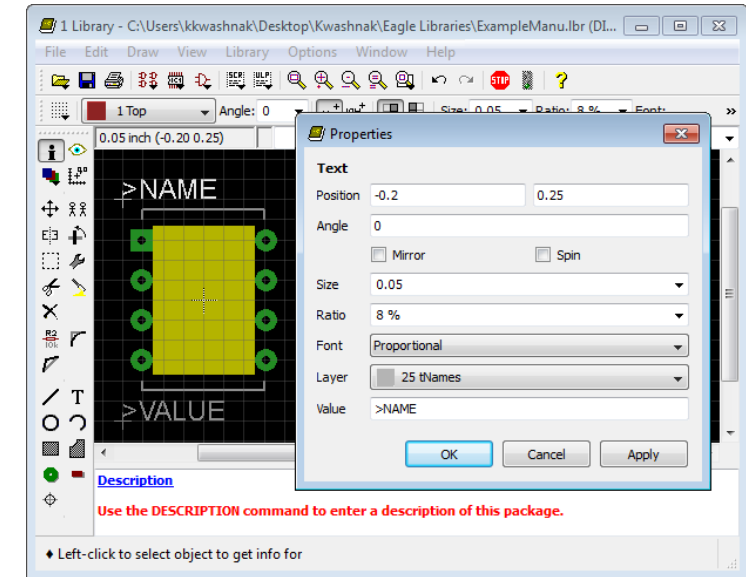
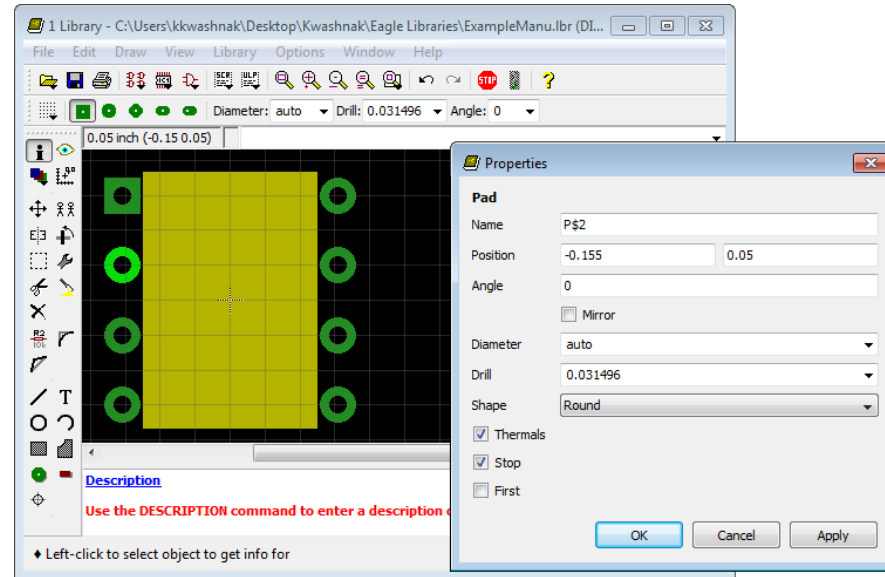
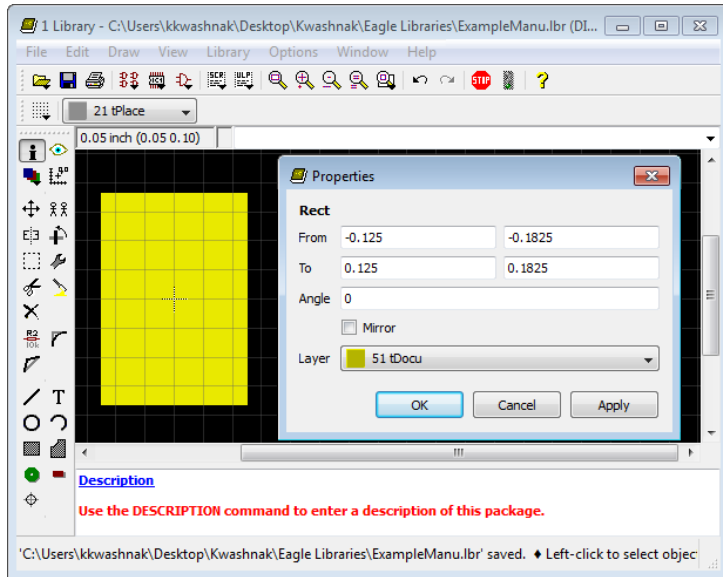
Creating a Component (Device) - Symbol

- The symbol should be designed first and referenced from the datasheet.
- Two main conventions for symbols:
 1. Ordered - looks exactly like the pinout of the device.
 2. Functional - pins are associated to their respective type of signal.
- Draw the component outline, add pins, and define all pin properties.



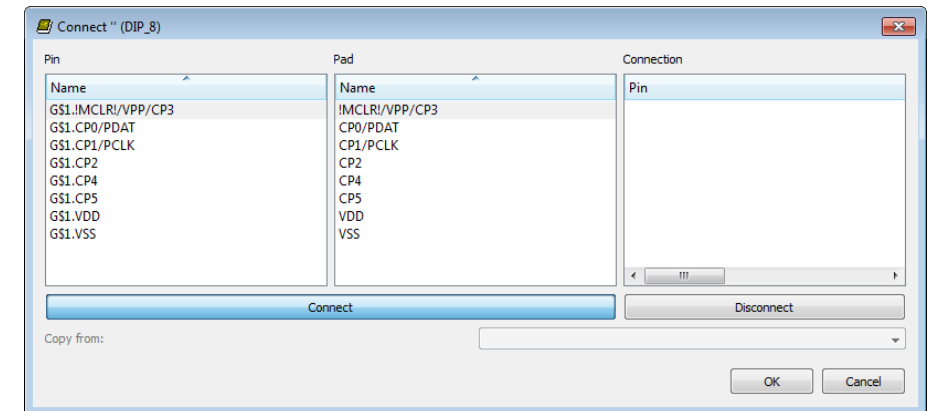
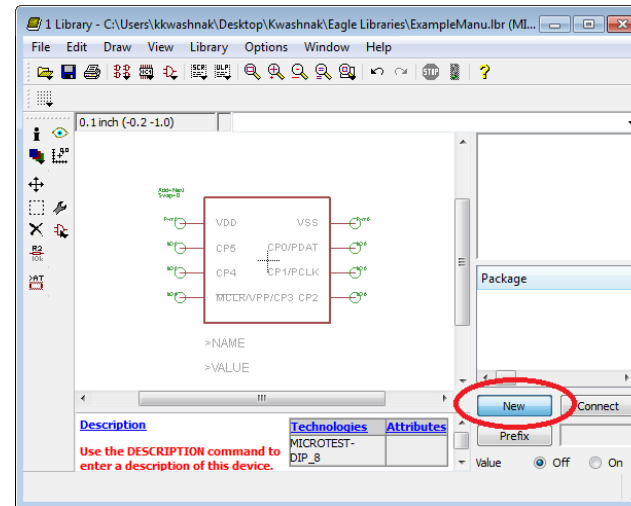
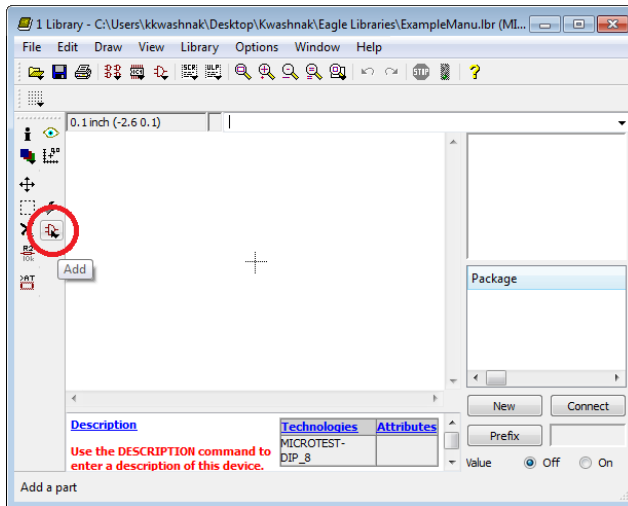
Creating a Component (Device) - Package

- The package will have multiple defined layers:
 - Silkscreen - component outline and labels (29 tPlace, 22 bPlace, 25 tNames, 26 bNames)
 - Pin holes/drills (44 drills, 45 holes)
 - Restriction zones
 - Clearance areas
- Draw the component body outline, add pins, configure pin properties, add text, and outline info.

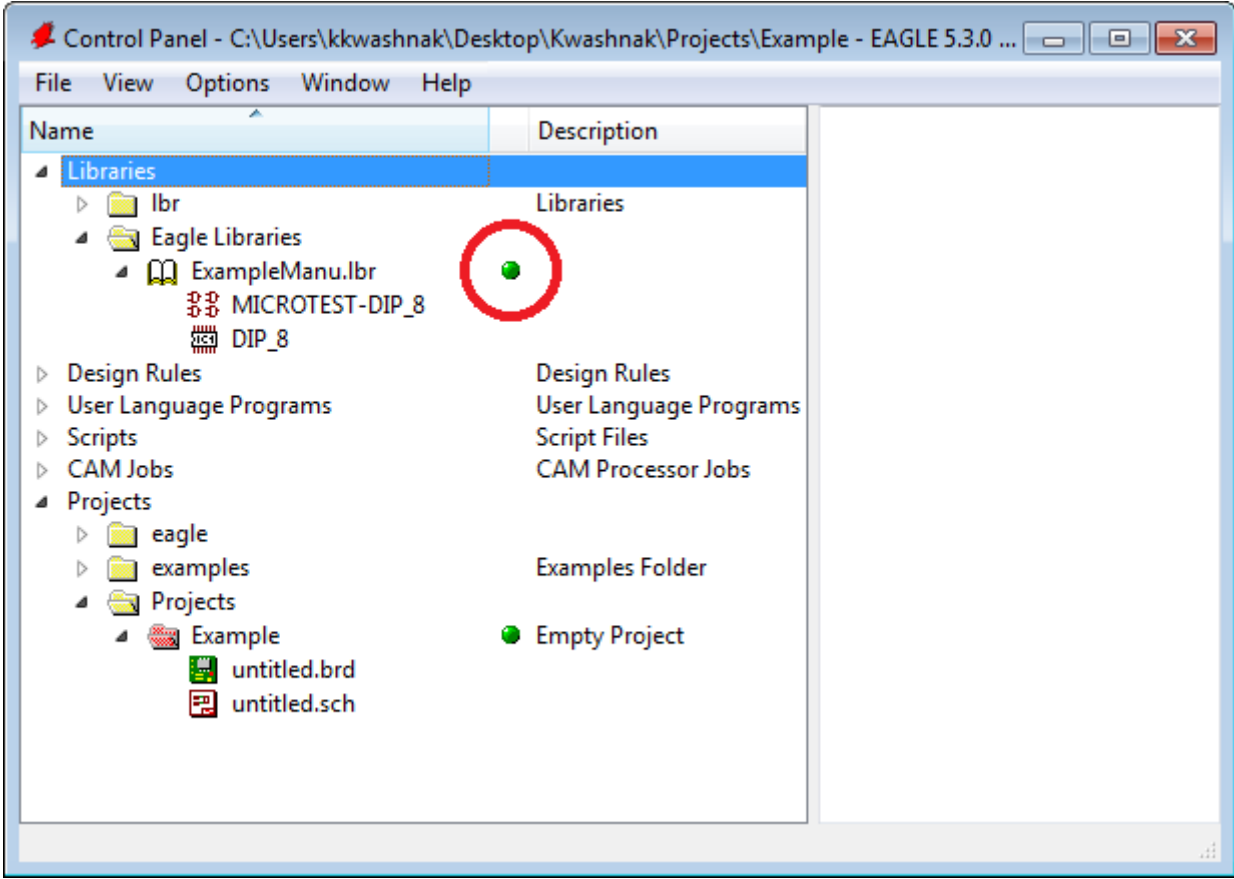


Creating a Component (Device) - Device

- Compiles symbol and package data into one object
- Allows creation of part variations
- Adds descriptions (in HTML format)
- Adds/places symbol, creates a new package, and associates connections (pins to pads)

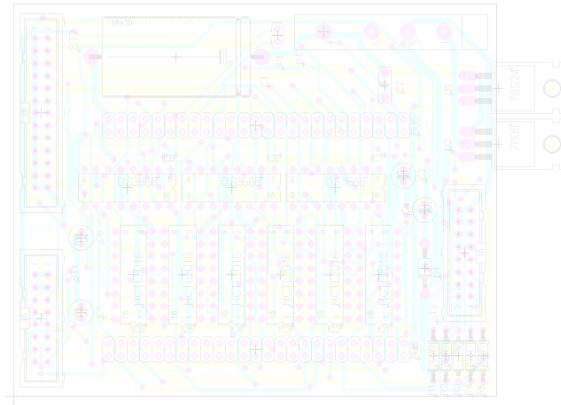


Creating a Component (Device) - Activate Library



Agenda

- Introduction



- Setup

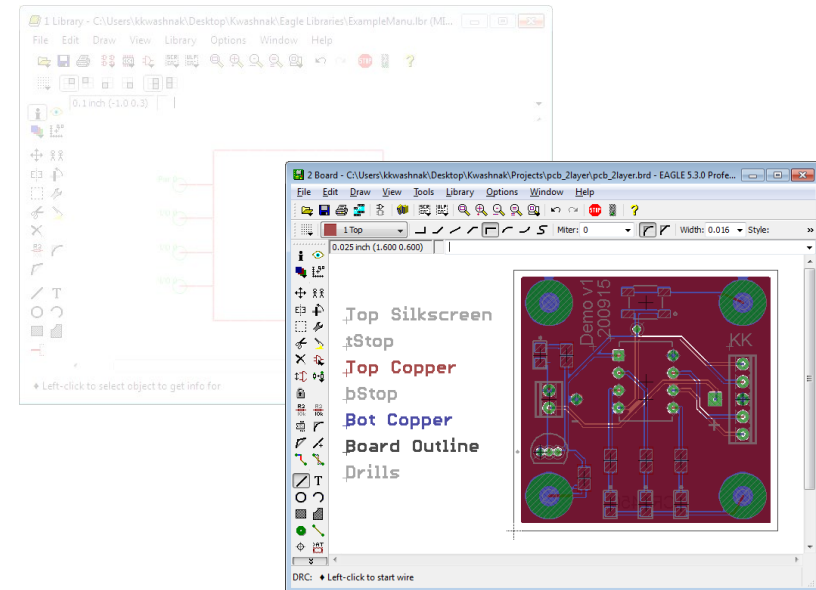


- Creating a Component (Device)

- Two-Layer PCB Design

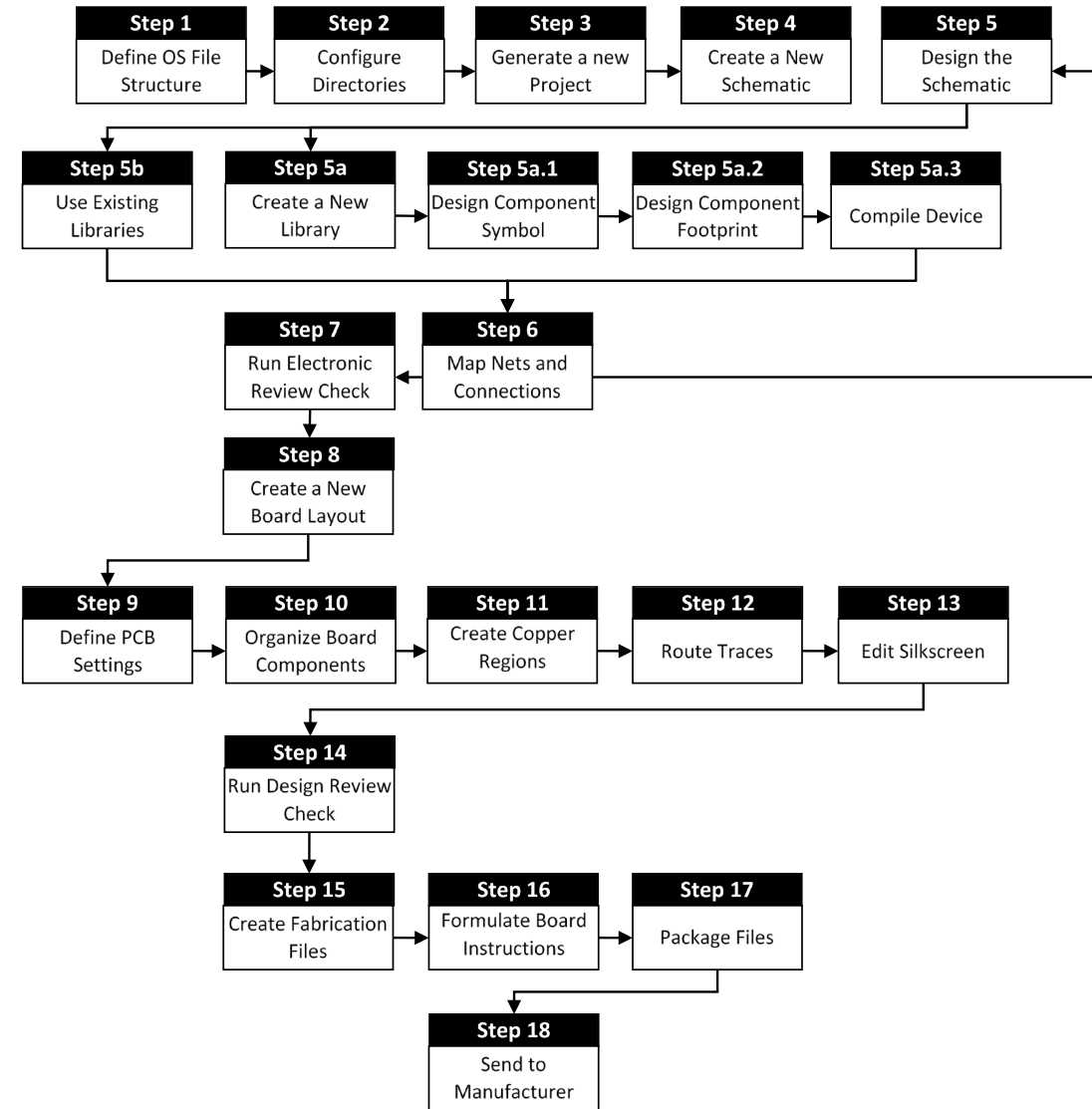


- Discussion

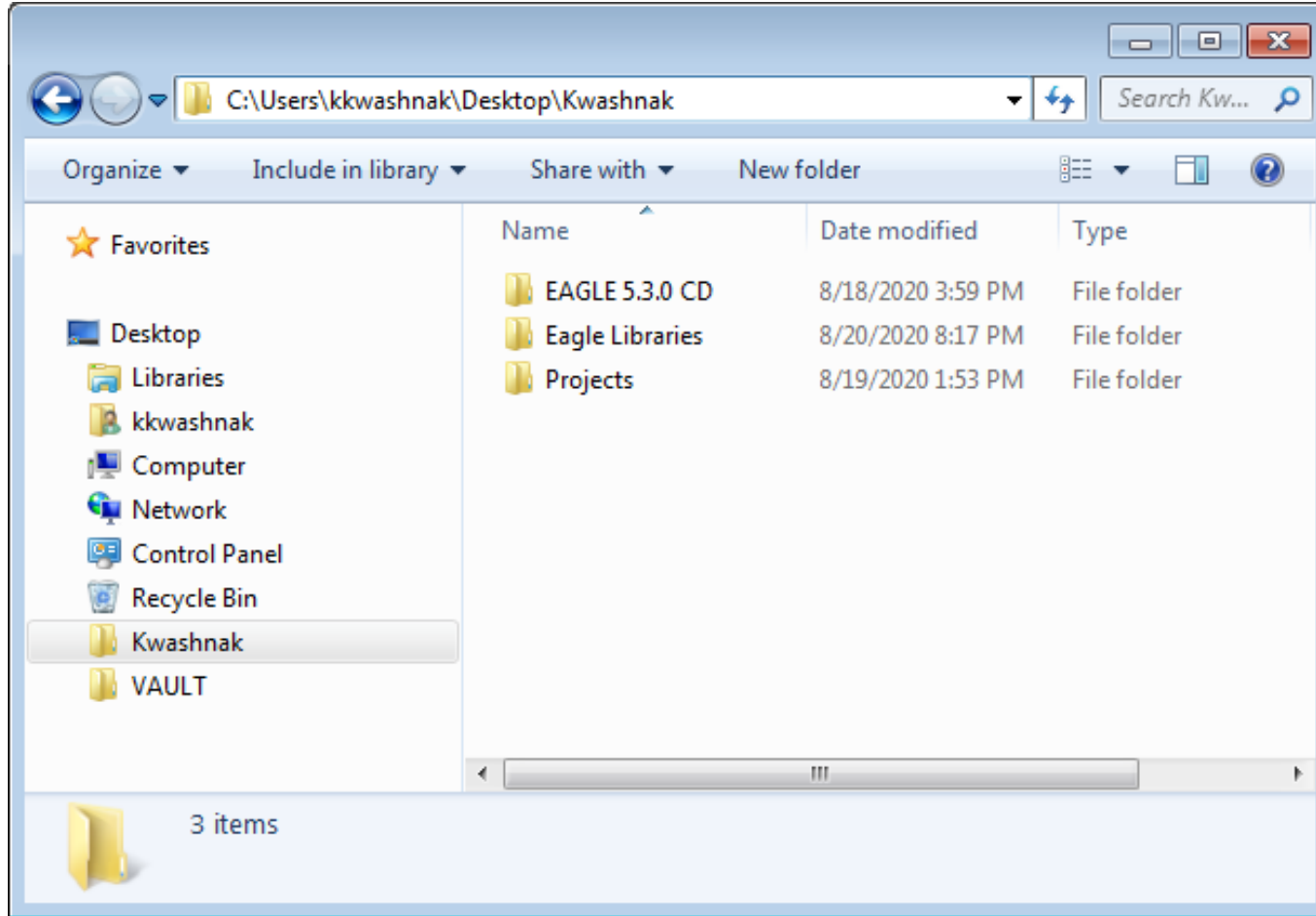


Two-Layer PCB Design

- Goal is to design a microcontroller board that will control three LEDs.
- Requirements:
 - **Dimensions:** about 1.5 inches x 1.5 inches x 0.0625 inches (length x width x height)
 - **Lead Free:** yes
 - **Material:** FR4
 - **Board Color:** green
 - **Copper Weight:** 1 oz
 - **Silkscreen Color:** white
 - **Silkscreen Placement:** top layer only (although design may have text on bottom layer)
 - **Plated Through Holes:** yes



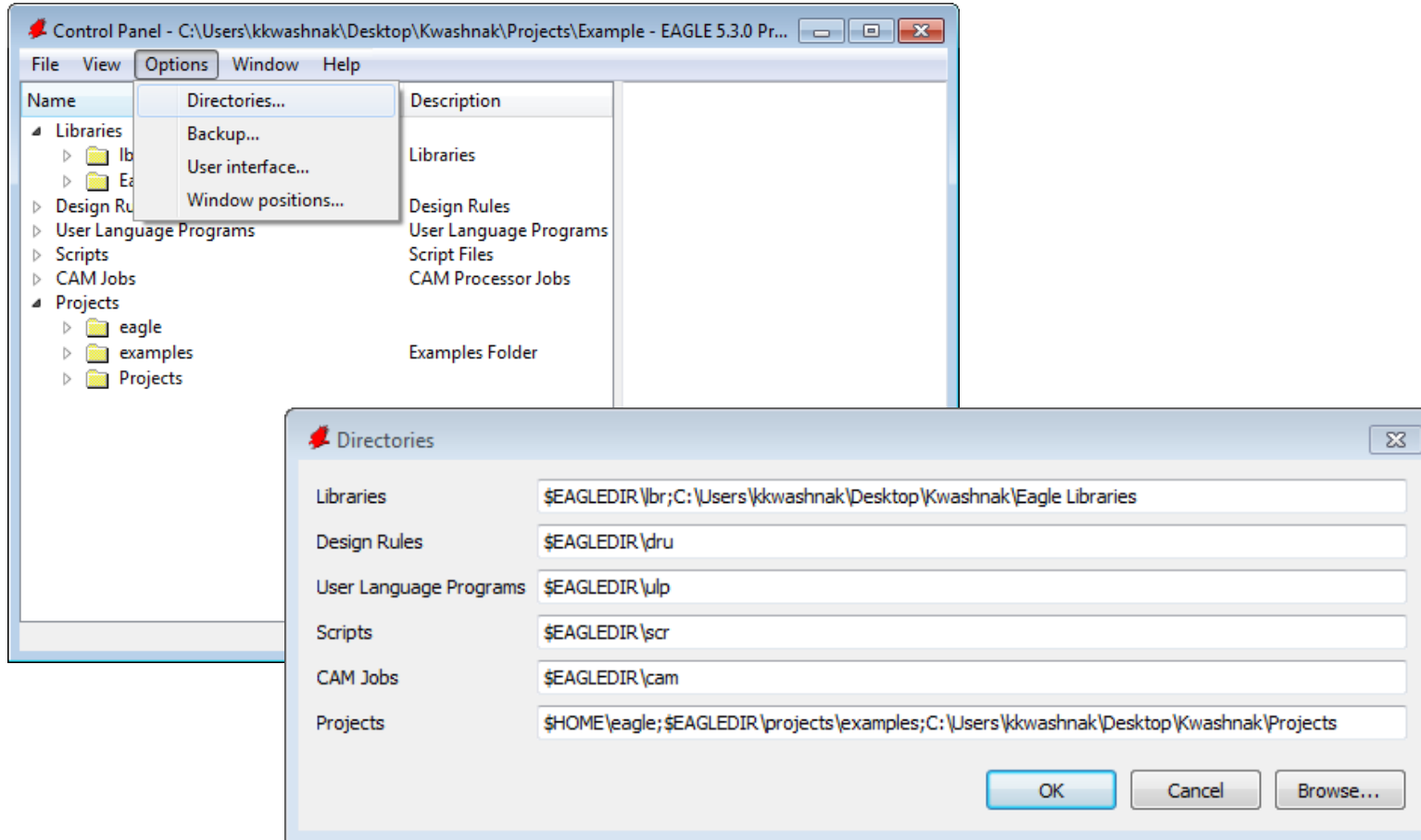
Two-Layer PCB Design - Step 1: OS File Structure



Create folders that will house project:

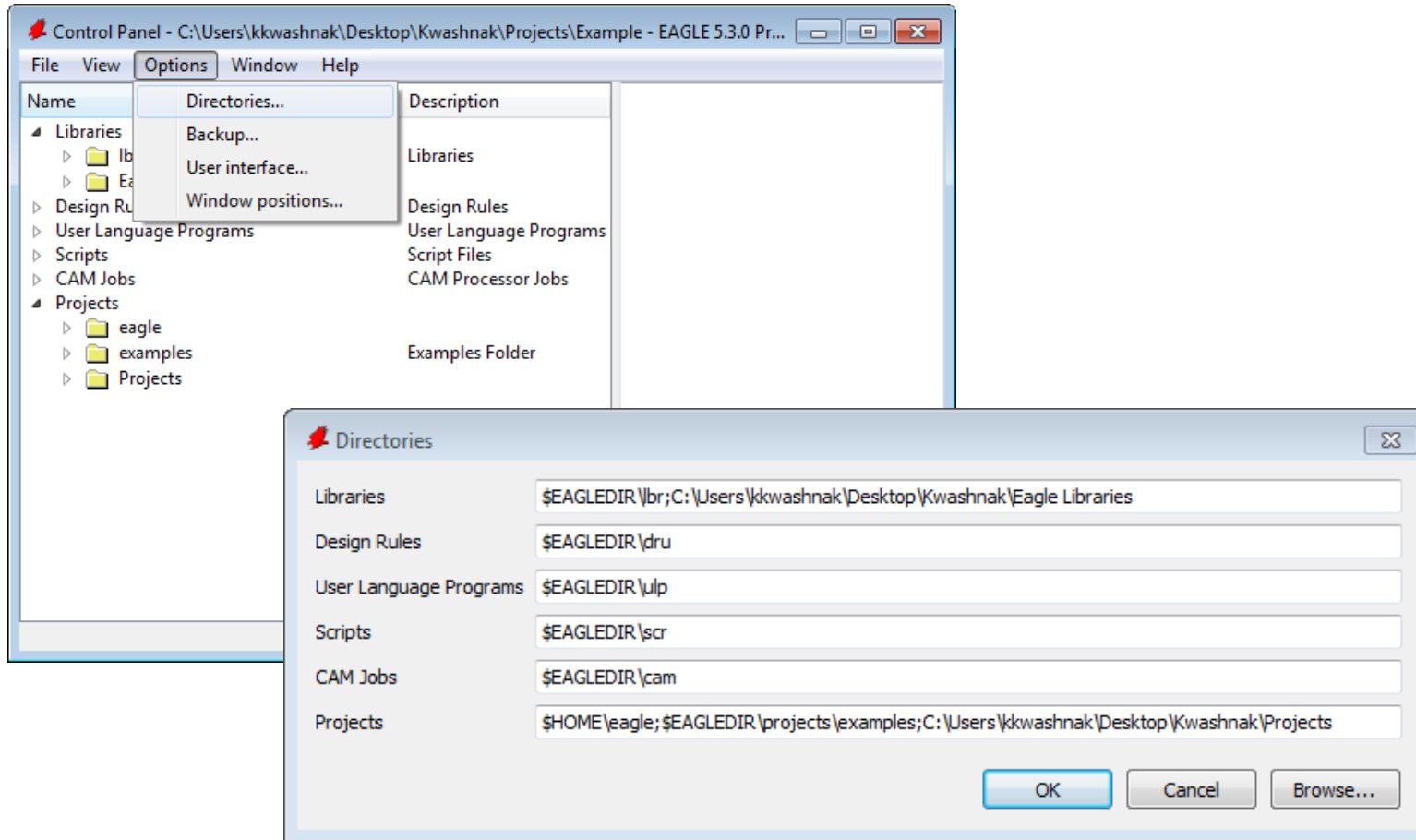
- Library
 - Schematic
 - Board
 - References
 - Design Rules
 - Fab
 - Notes
- Project

Two-Layer PCB Design - Step 2: Configure Directories



- Add location paths to EAGLE's directories
- Adding directories requires a ';' directly after the previous path; do not add a space before the next location

Two-Layer PCB Design - Step 3: Generate a New Project



Create folders that will house project

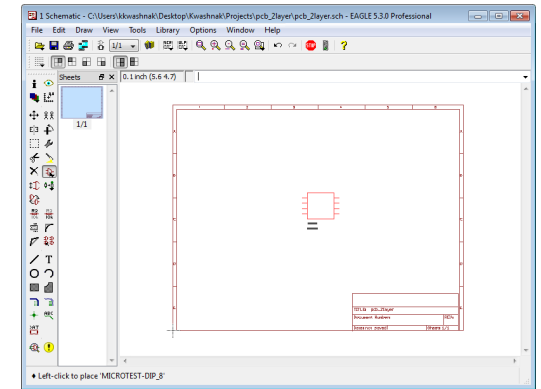
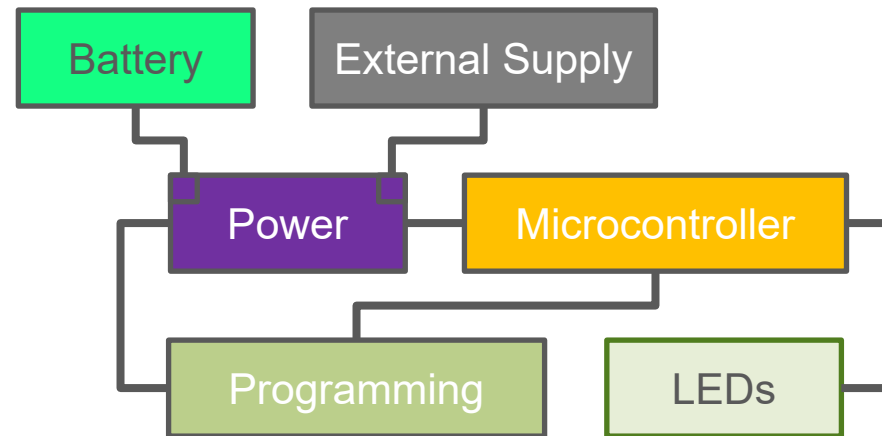
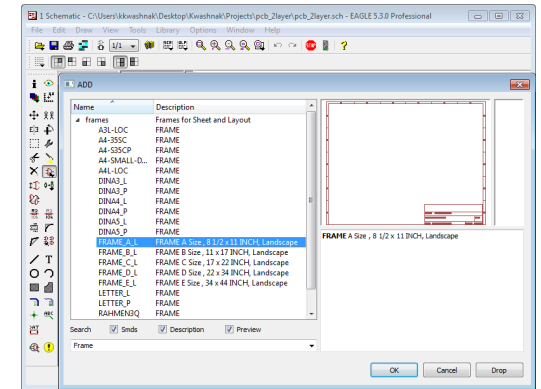
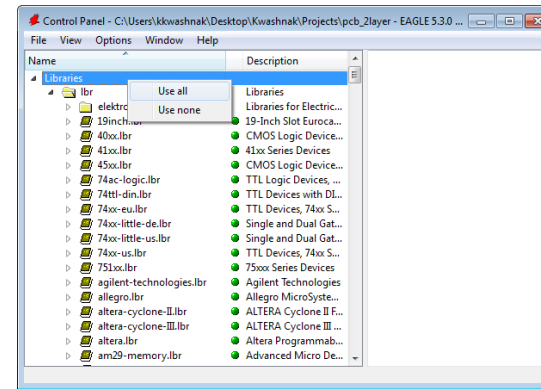
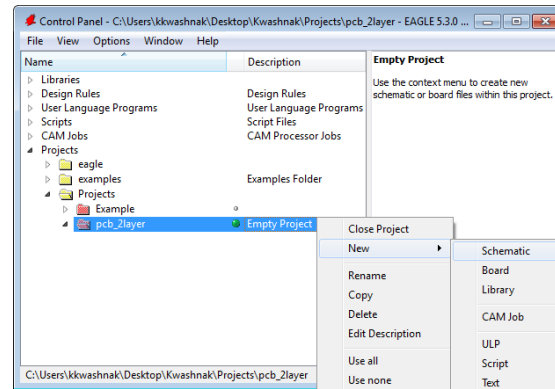
– Library

– Project

- Schematic
- Board
- References
- Design Rules
- Fab
- Notes

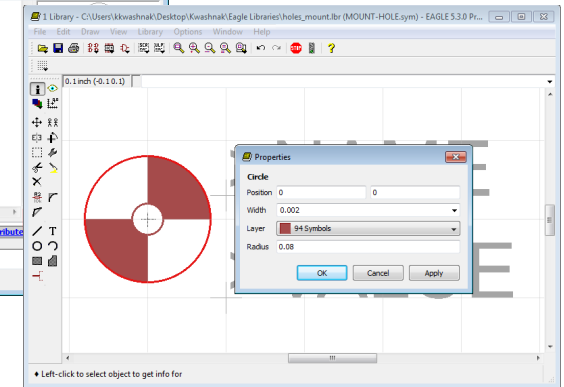
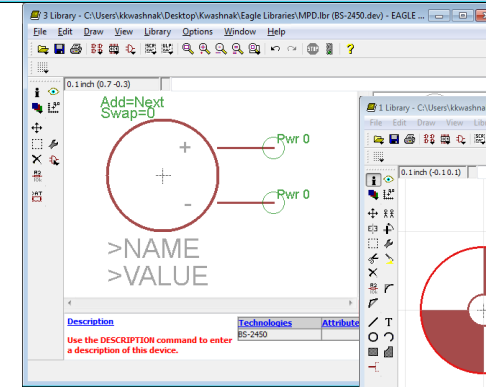
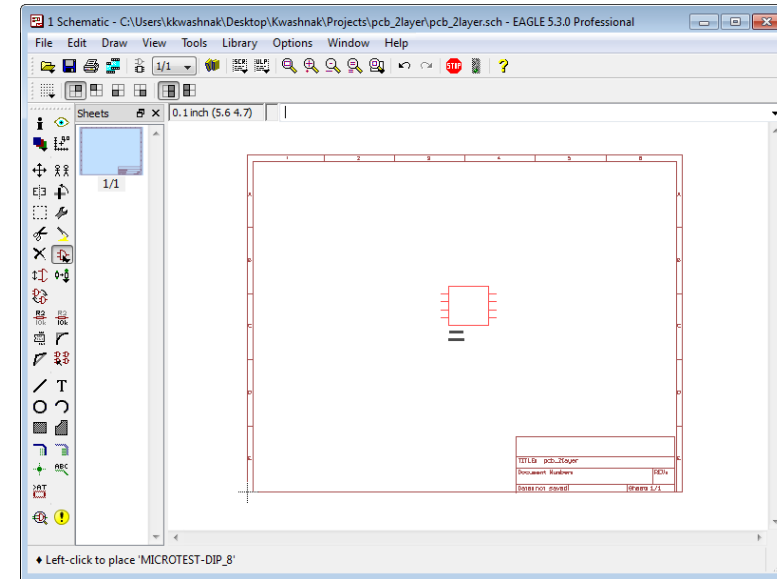
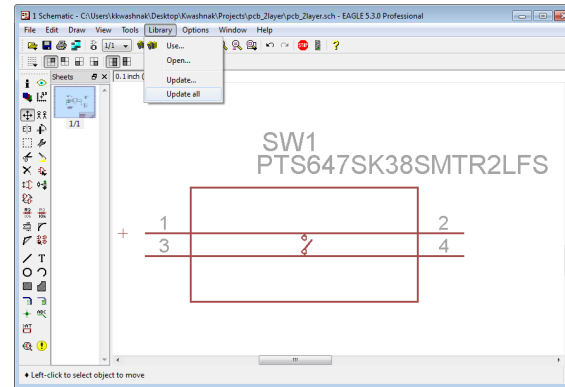
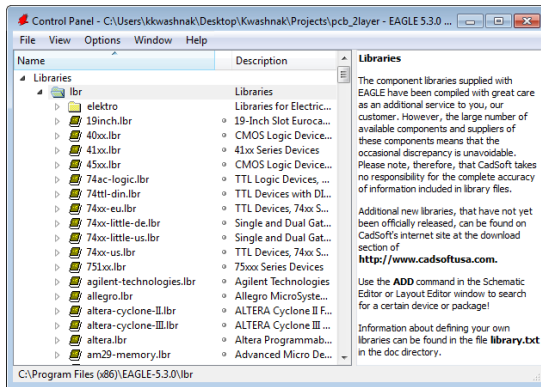
Two-Layer PCB Design - Step 4: Create a New Schematic

- Research components
- Create a new schematic
- Formulate a systems diagram
- Activate/create libraries
- Diagram circuit
- Create Bill of Materials (BOM)



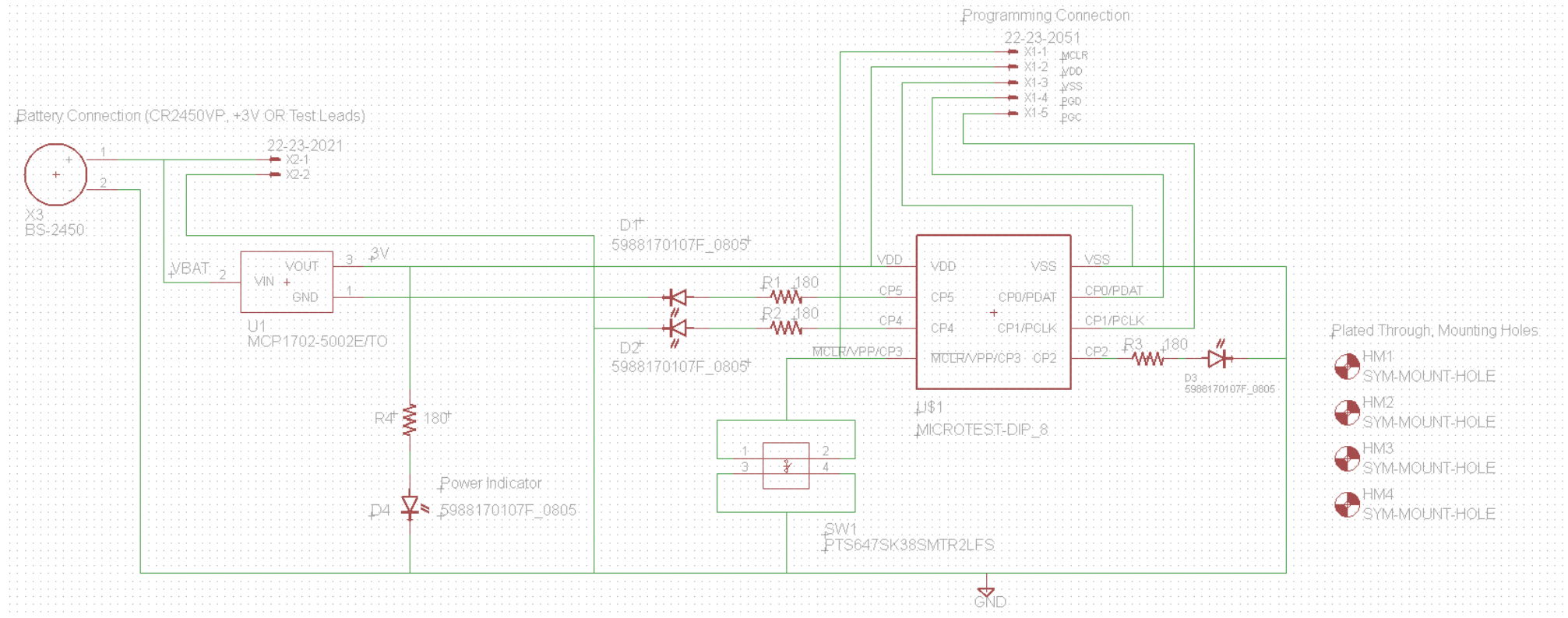
Two-Layer PCB Design - Step 5: Design the Schematic

- Populate schematic with components
- Roughly place and organize hardware
- Use existing libraries
- Import libraries
- Modify existing devices (variants)
- Create new library
 - Device
 - Symbol
 - Package/footprint



Two-Layer PCB Design - Step 6: Map Nets and Connections

Sch Editor



- Organize components
- Name nets

- Add labels to describe system
- Add nonlinked devices

Two-Layer PCB Design - Step 7: Run Electronic Review Check

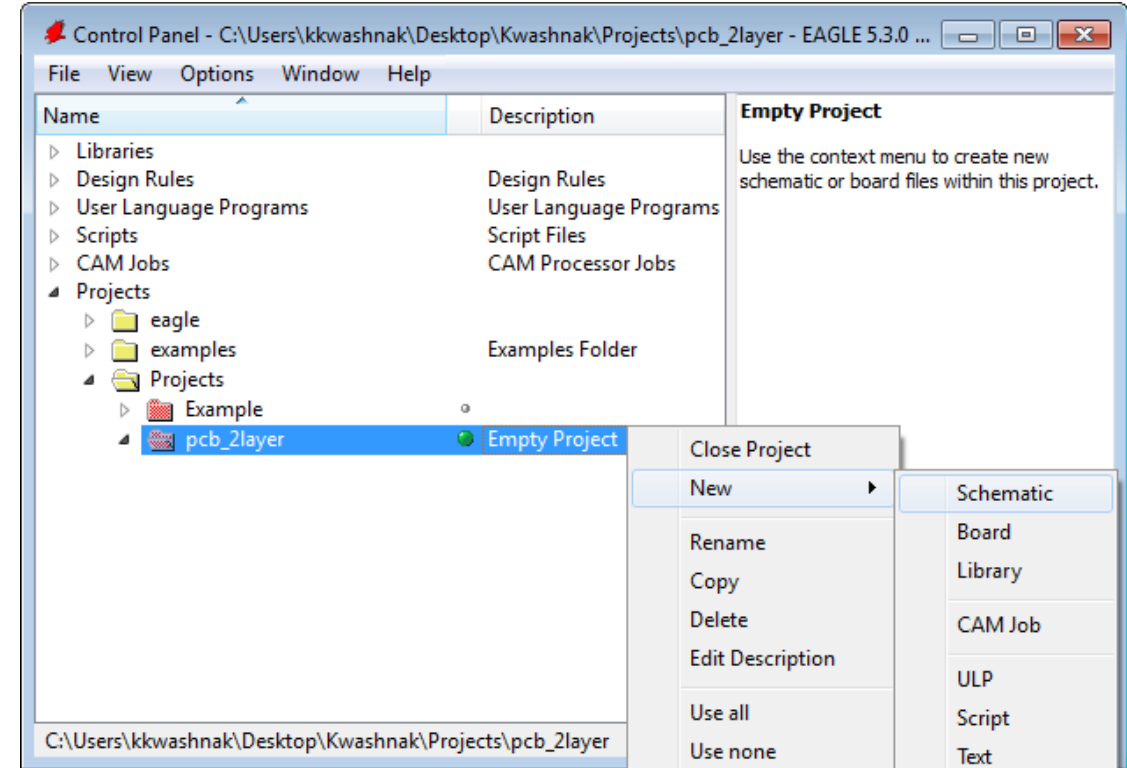
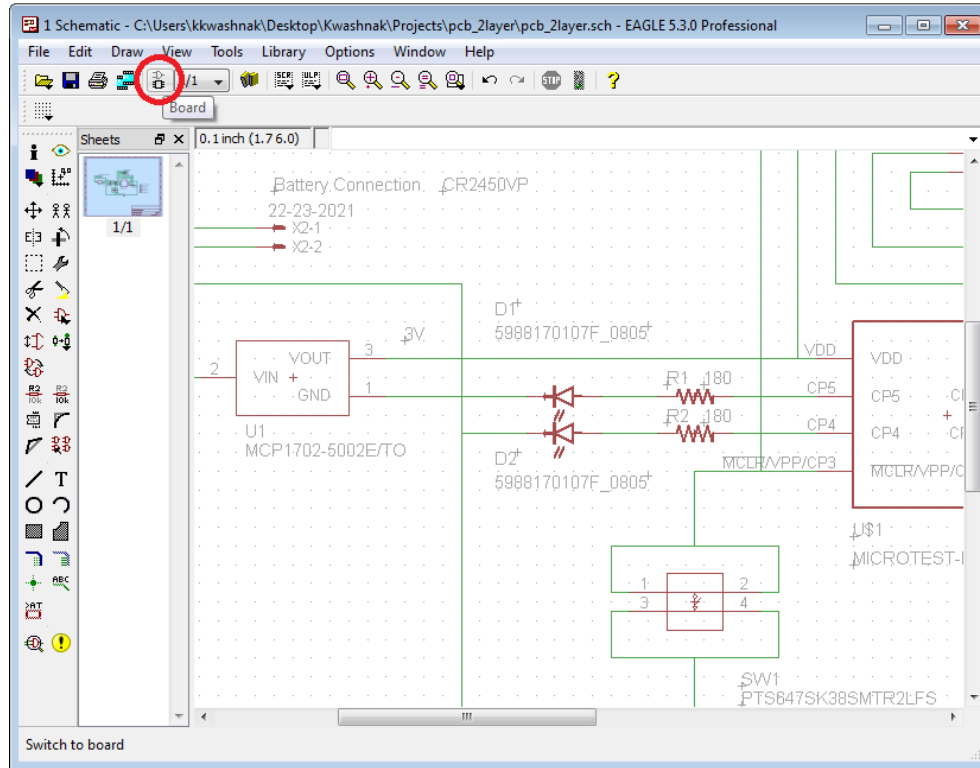
The screenshot displays the Eagle PCB design environment. The main window shows a schematic diagram of a PCB layout with various components and their interconnections. A black arrow points from a specific component in the schematic to the 'Missing junction in net NS20' warning in the 'ERC Errors' dialog box. The dialog box lists 41 warnings, including missing junctions in various nets and unintended grounding of nets. The status bar at the bottom left indicates 'ERC: finished (41 errors/warning)'. A title block in the bottom right of the schematic area contains the following information:

Ken Kuashnak	
SERVICE Engineering Company	
TITLE: pcb_2layer	
Document Number:	REV:
198731 Demo Microcontroller Board	1
Date: 9/15/2020 3:58:00 PM	Sheet: 1/1

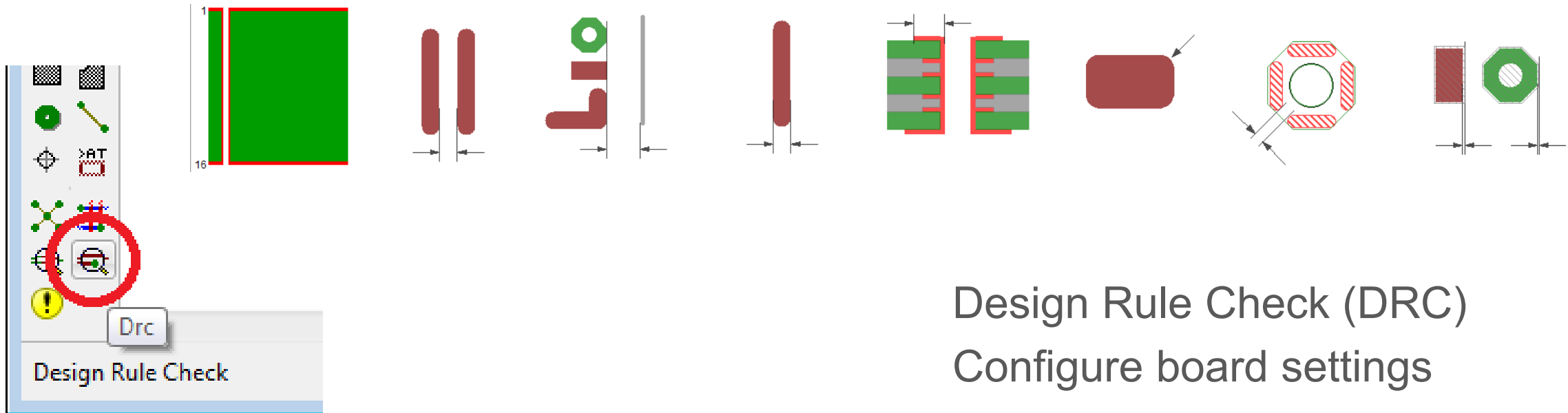
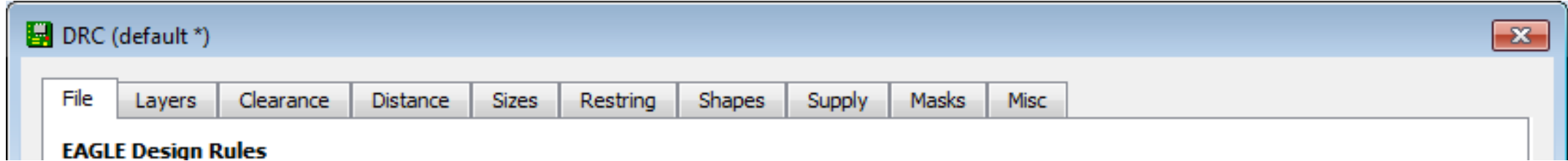
Check schematic for errors:

- Pin-type assignments
- Missing connections
- Unintended grounding of nets
- Connection diagramming

Two-Layer PCB Design - Step 8: Create a New Board Layout



Two-Layer PCB Design - Step 9: Define PCB Settings



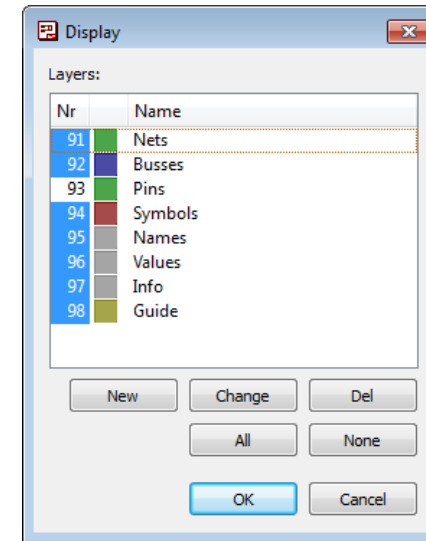
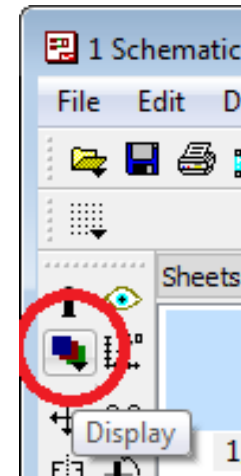
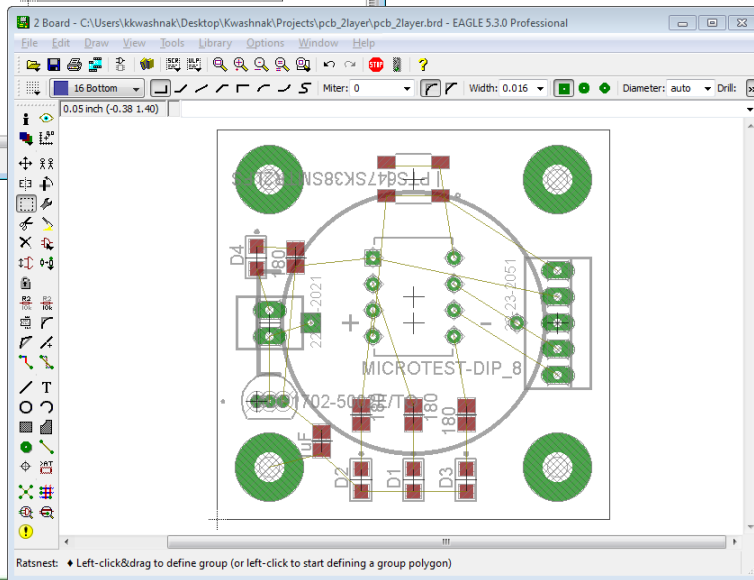
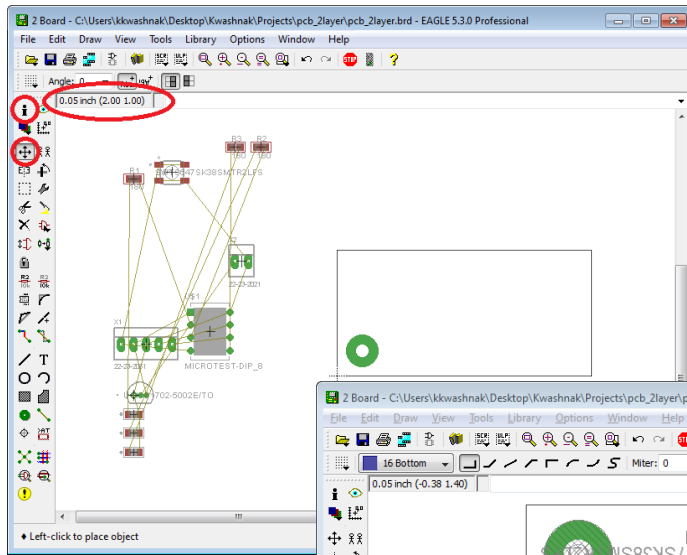
Two-Layer PCB Design - Step 10: Organize Components

Brd Editor

- Lay out components.
 - Be aware of assembly process!
 - Be aware of silkscreen placement!
- Review air wires.
- Configure board dimension.
- Schematic dictates devices on board.

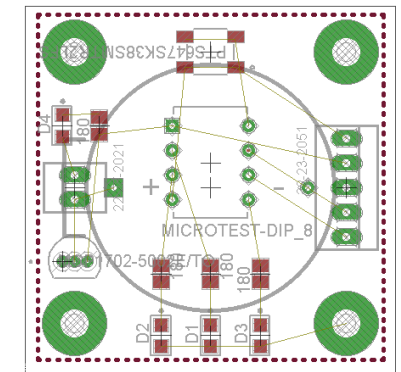
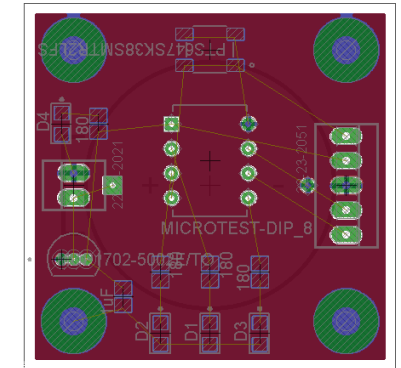
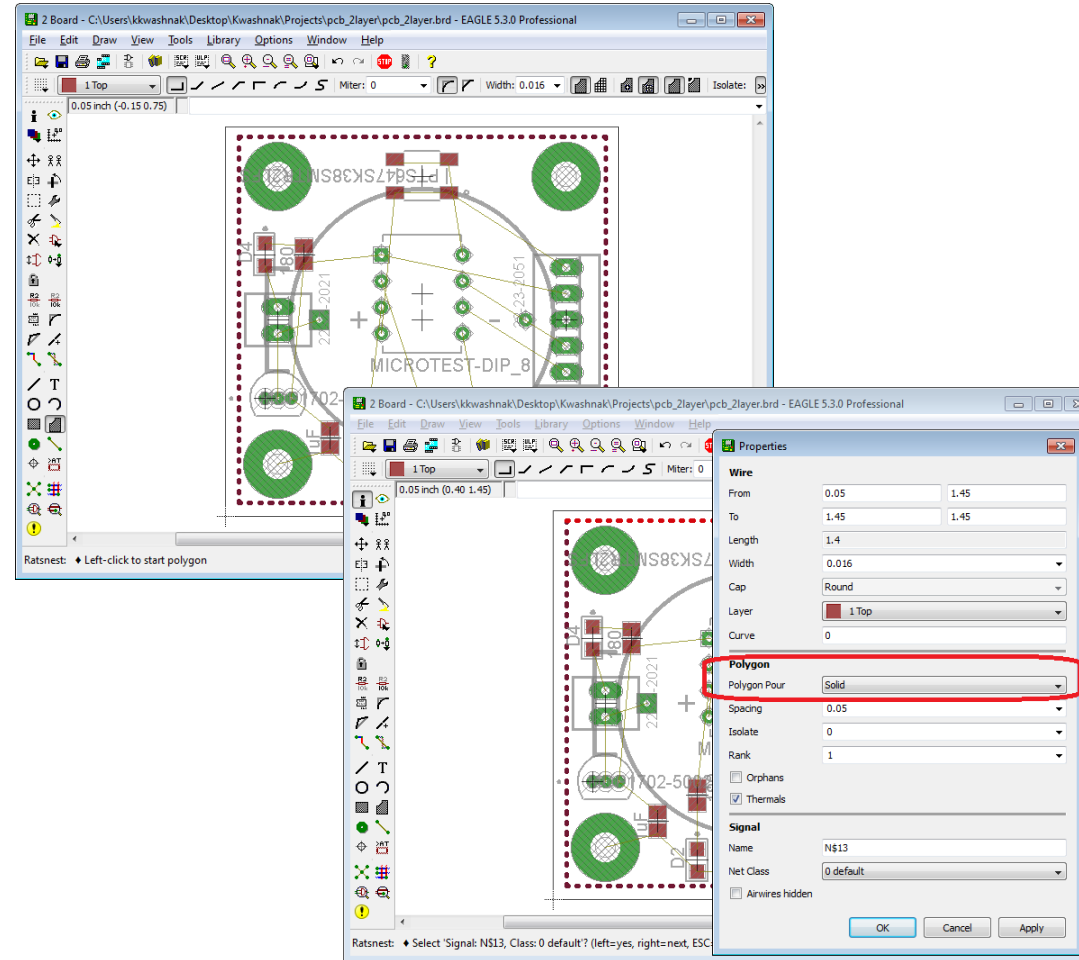
Use <Info> tool often to check object properties.

- Make sure objects are on the correct layer.

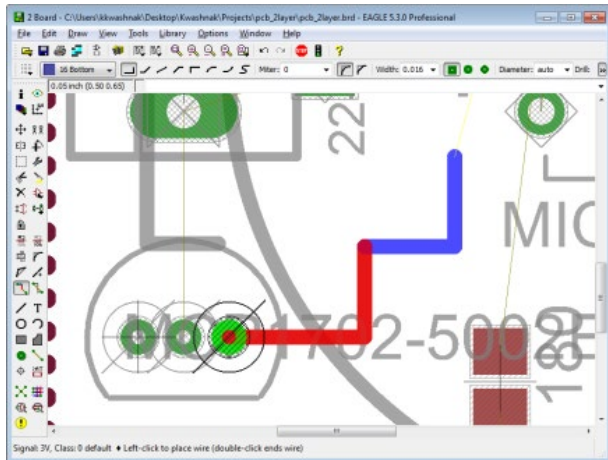
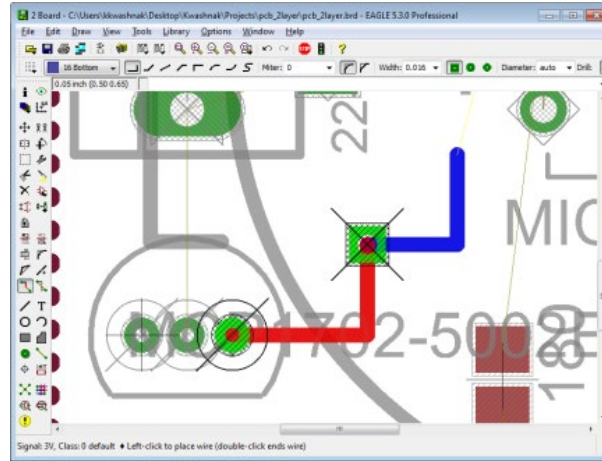
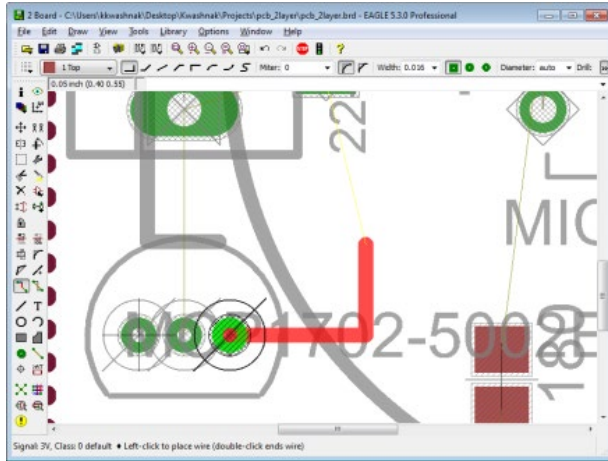


Two-Layer PCB Design - Step 11: Create Copper Regions

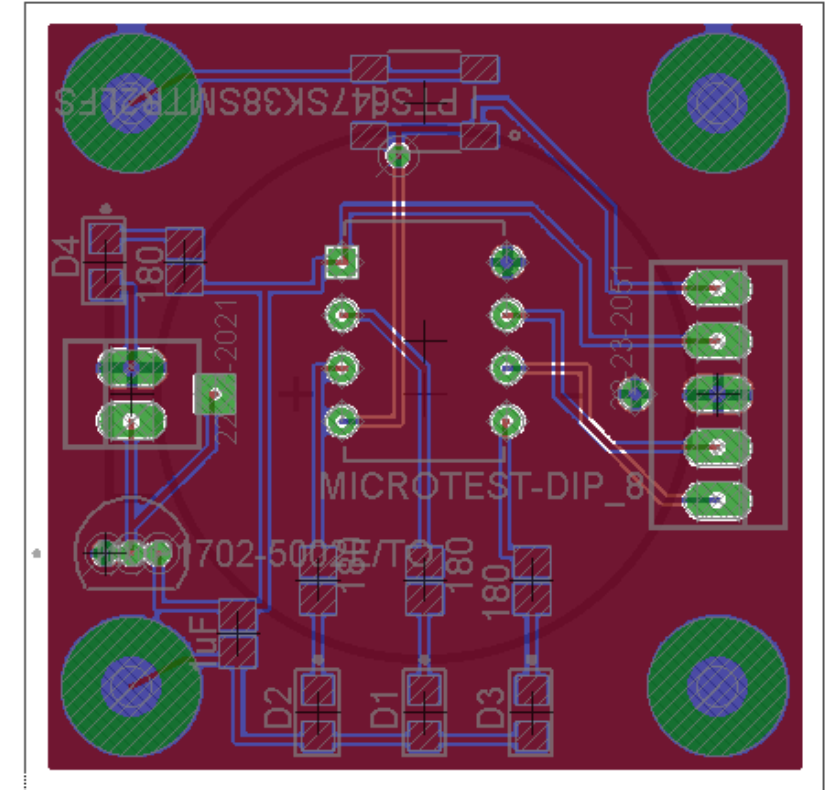
- Create an area on the board where copper will be poured.
- Configure region settings.
- Regions will be on top and bottom of the board.



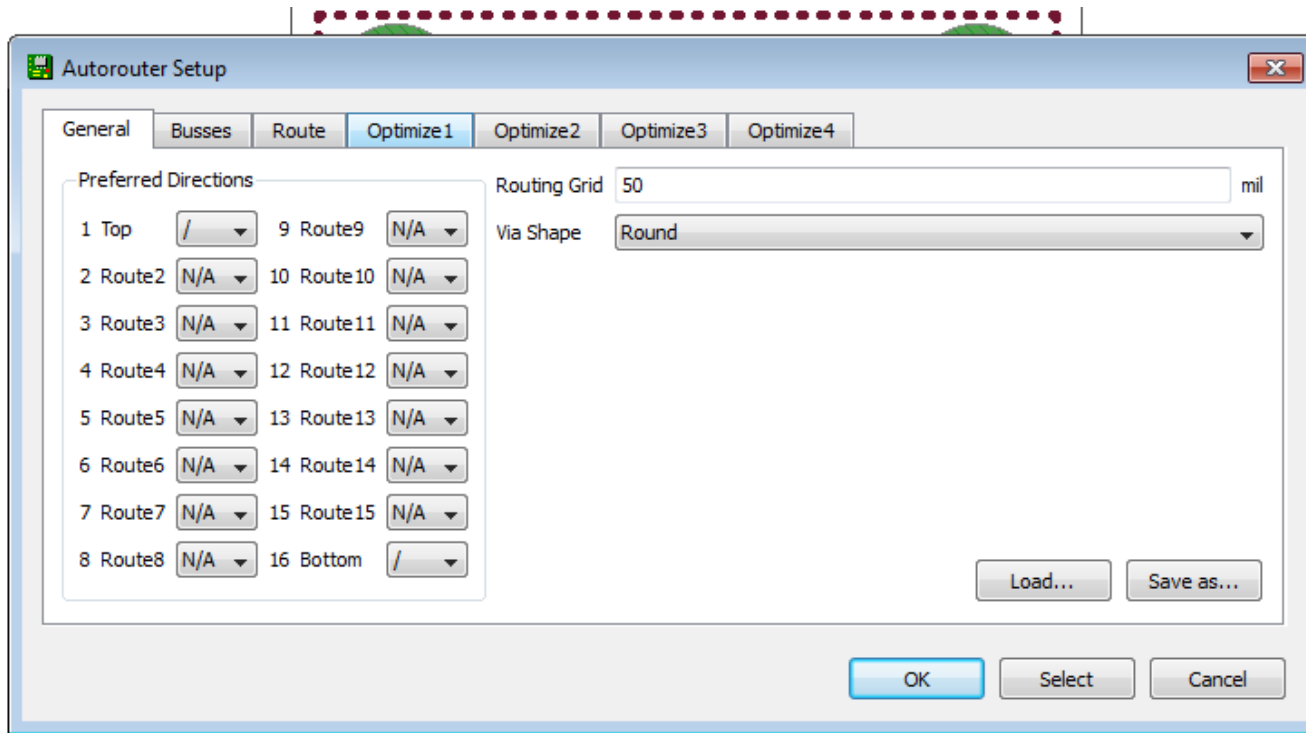
Two-Layer PCB Design - Step 12: Route Traces



- Use air wires as a reference
- When routing, change layers with layer dropdown to go from top to bottom of the board (creates a Via)
- When routing, right-click cycles through wire type
- Auto-router



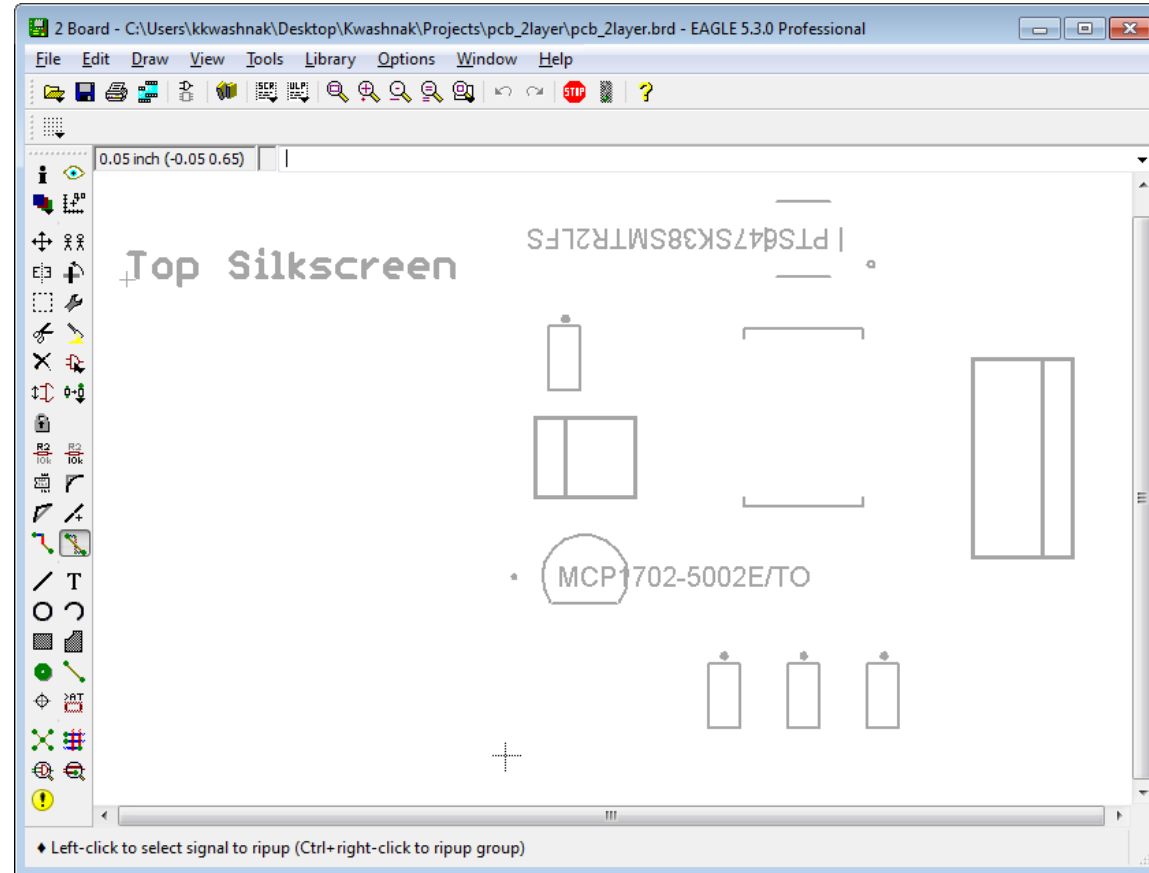
Two-Layer PCB Design - Step 12: Route Traces (cont.)



Symbol	Preferred Direction
-	Left to Right
	Up and Down
/	45 deg, Bottom Left to Top Right
\	45 deg, Top Left to Bottom Right
*	No Preference
Auto	EAGLE will access and optimize

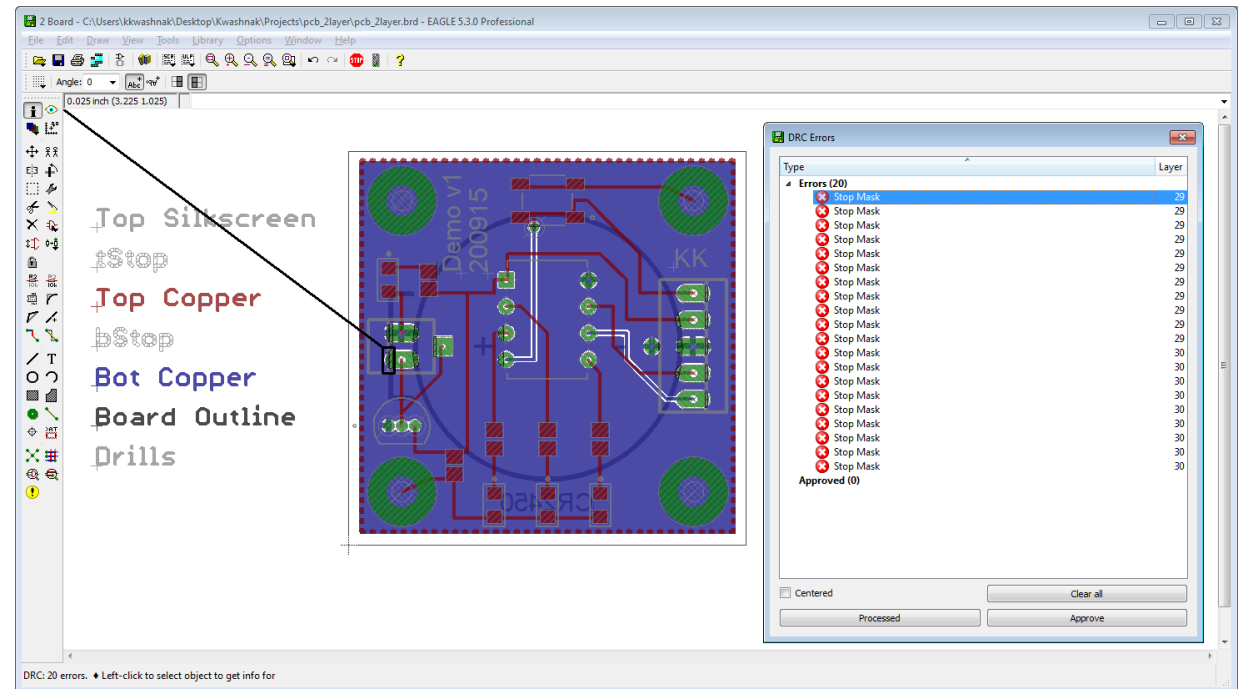
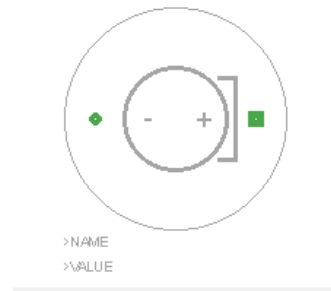
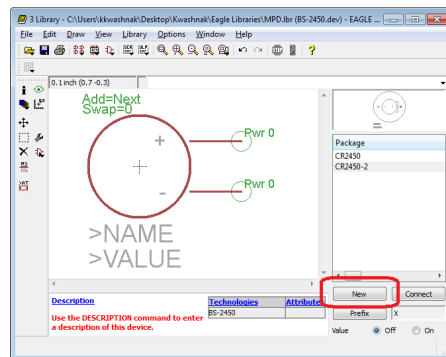
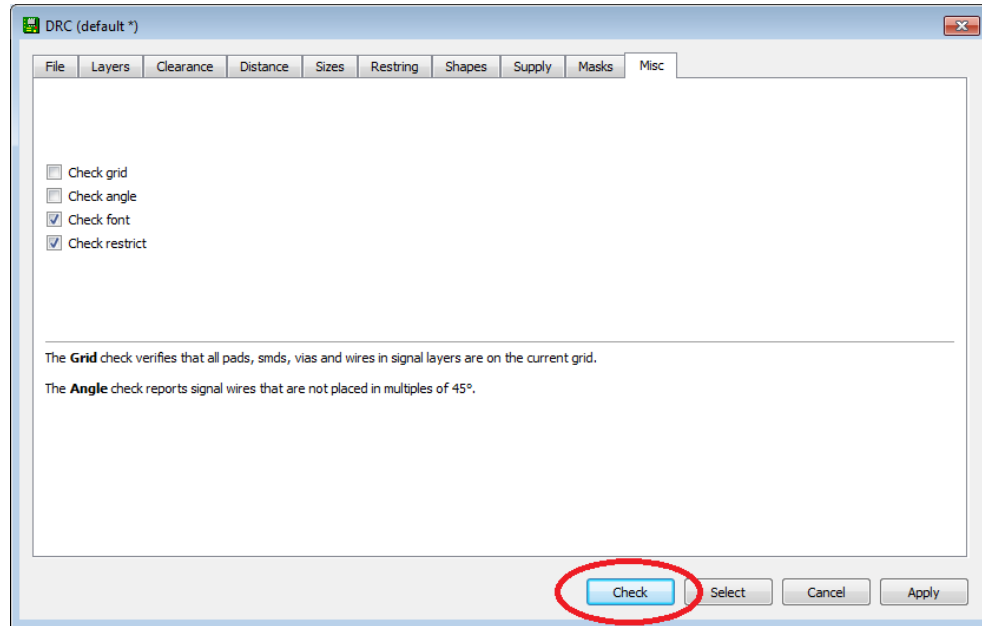
Two-Layer PCB Design - Step 13: Edit Silkscreen

- 21 tPlace,
- 22 bPlace
- 25 tNames
- 26 bNames
- <Text> tool
 - Either layer
'21 tPlace' or
'22 bPlace'
- Helpful to turn
on/off layers



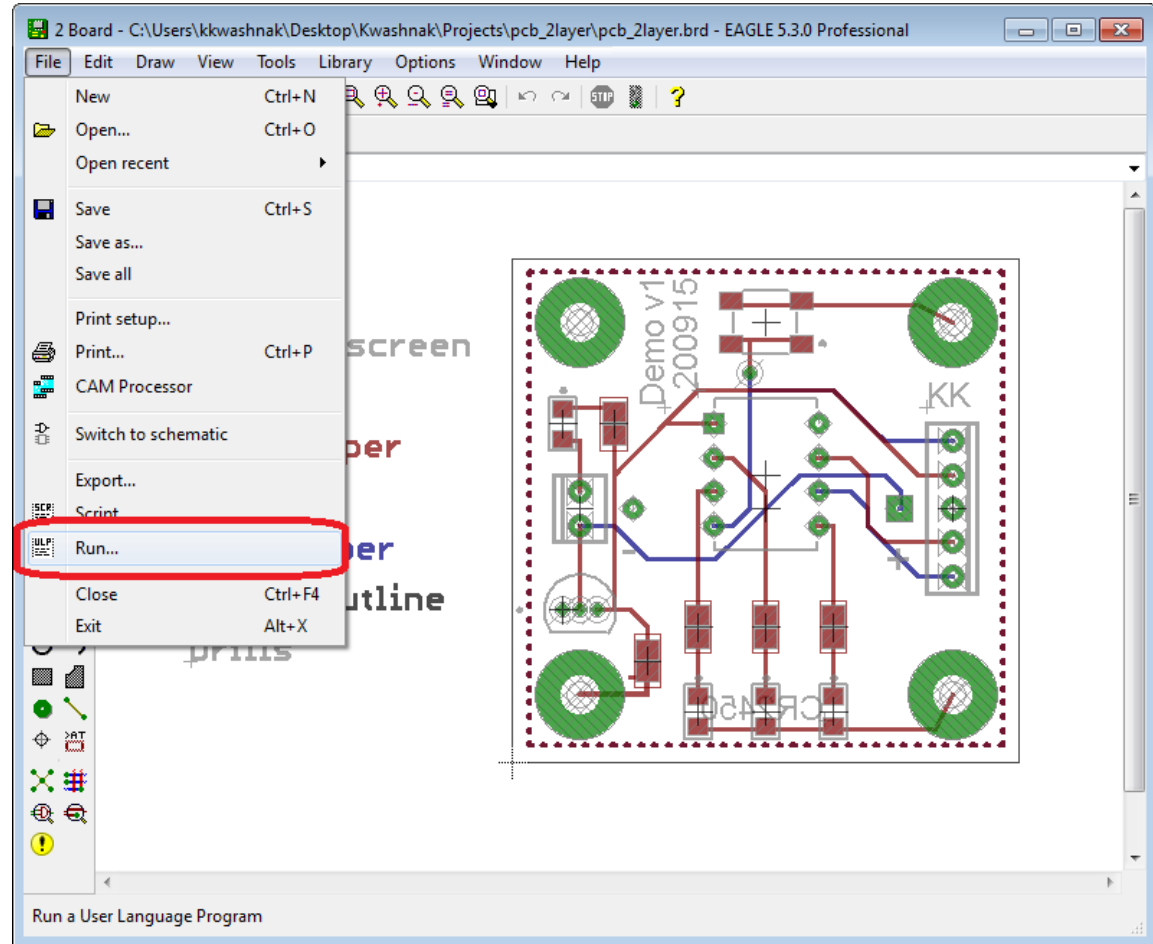
Two-Layer PCB Design - Step 14: Run Design Review Check

- DRC might find numerous warnings or errors
- Silkscreen symbols might interfere with pin holes.
 - Change board requirements
 - Change symbol (create a variant)



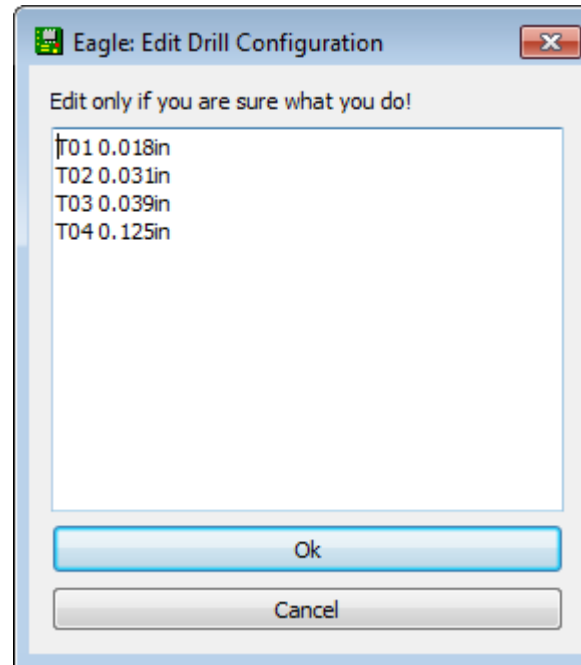
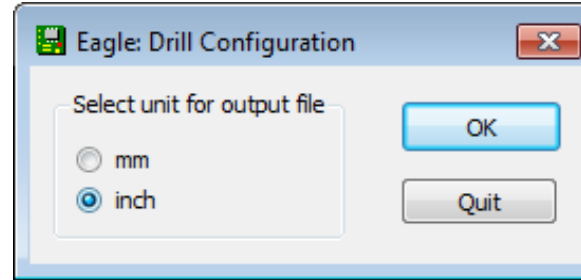
Two-Layer PCB Design - Step 15: Create Fabrication Files

- ULPs
 - drillcfg.ulp
 - Configures drill holes
- CAM Processor
 - excellon.cam
 - Generates drill data
 - gerb274x.cam
 - Layers information



Two-Layer PCB Design - Step 15: Create Fabrication Files (cont.)

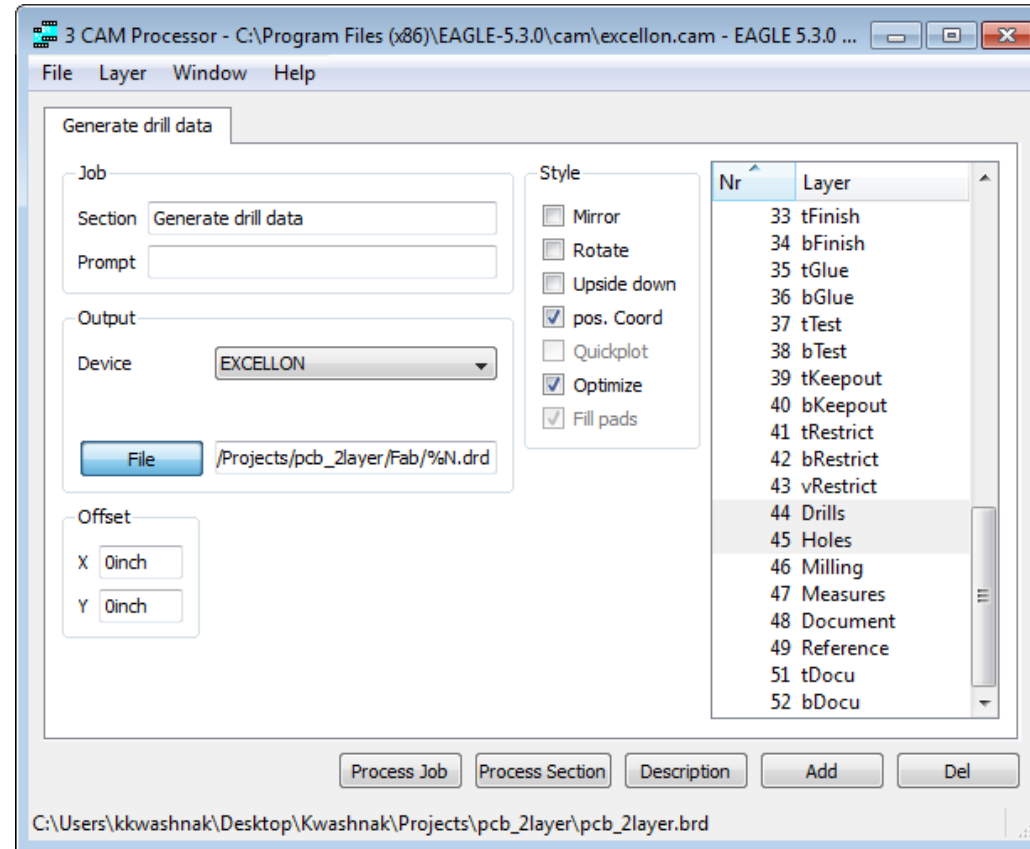
- ULPs
 - drillcfg.ulp
 - Configures drill holes
- CAM Processor
 - excellon.cam
 - Generates drill data
 - gerb274x.cam
 - Layers information



output = .drl

Two-Layer PCB Design - Step 15: Create Fabrication Files (cont.)

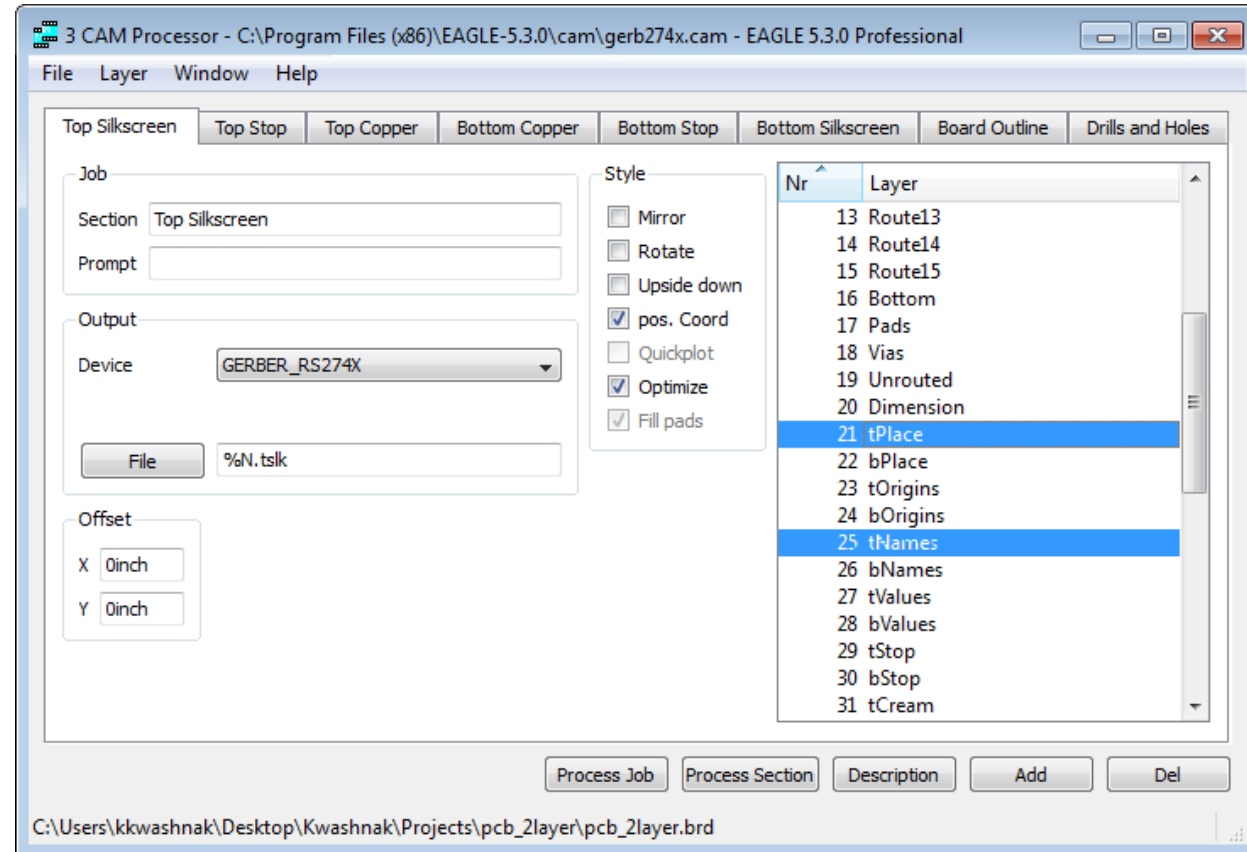
- ULPs
 - drillcfg.ulp
 - Configures drill holes
- CAM Processor
 - excellon.cam
 - Generates drill data
 - gerb274x.cam
 - Layers information



output = drd and .dri

Two-Layer PCB Design - Step 15: Create Fabrication Files (cont.)

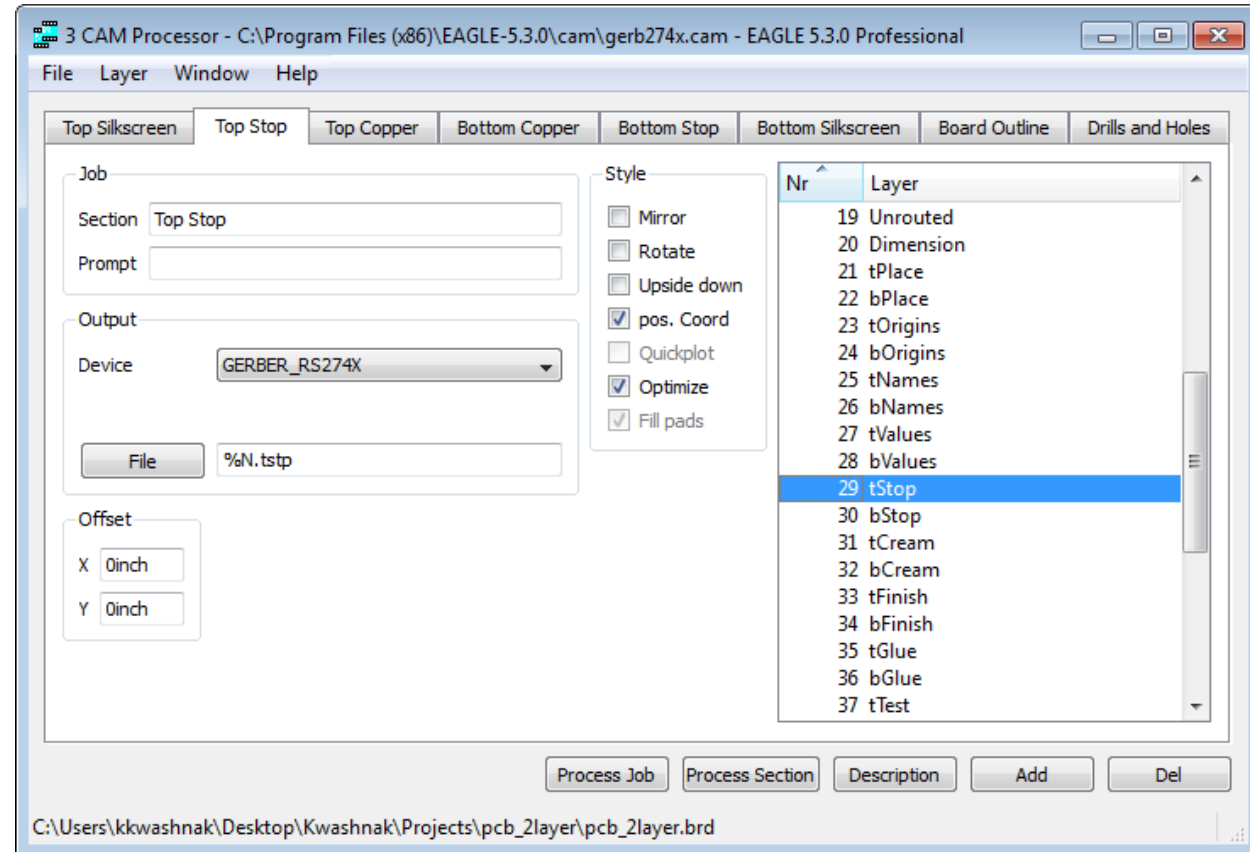
- ULPs
 - drillcfg.ulp
 - Configures drill holes
- CAM Processor
 - excellon.cam
 - Generates drill data
 - gerb274x.cam
 - Layers information



output = .tslk

Two-Layer PCB Design - Step 15: Create Fabrication Files (cont.)

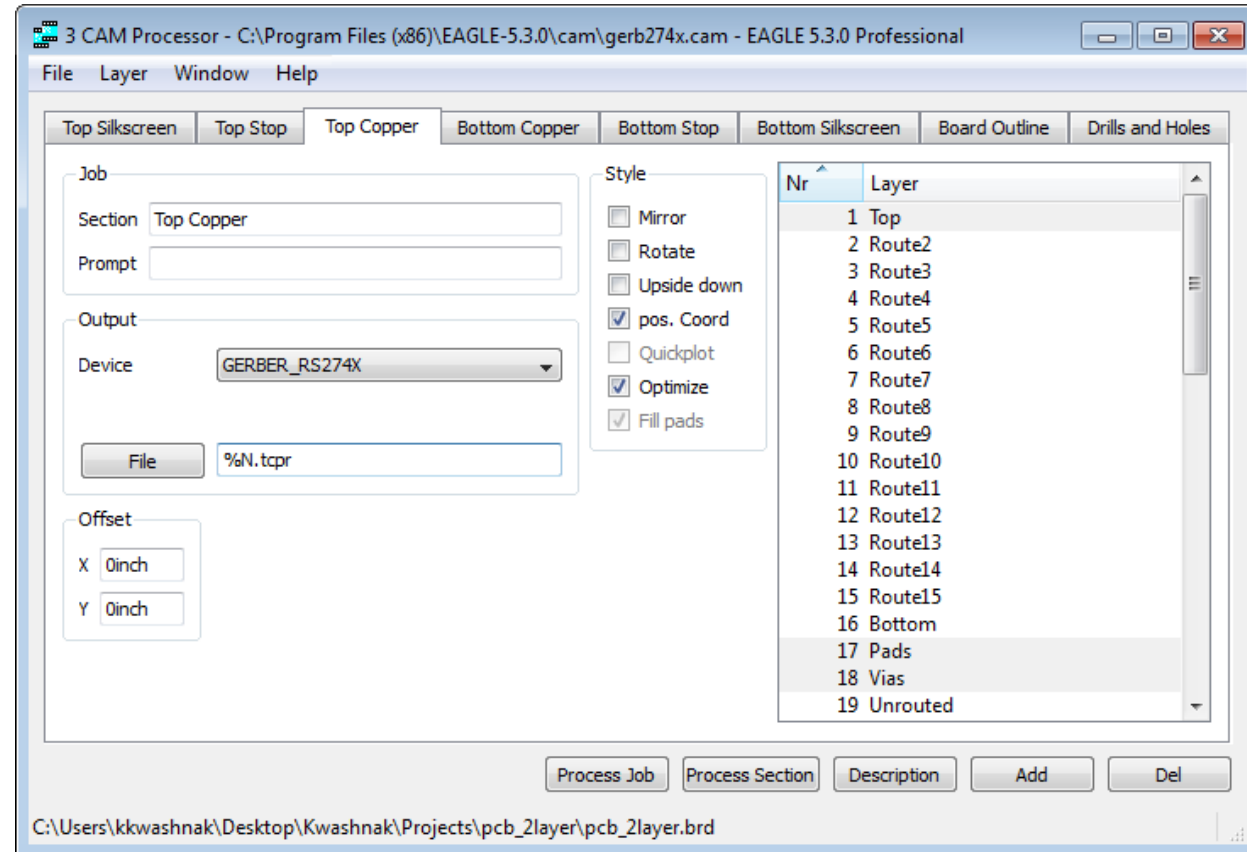
- ULPs
 - drillcfg.ulp
 - Configures drill holes
- CAM Processor
 - excellon.cam
 - Generates drill data
 - gerb274x.cam
 - Layers information



output = .tstp

Two-Layer PCB Design - Step 15: Create Fabrication Files (cont.)

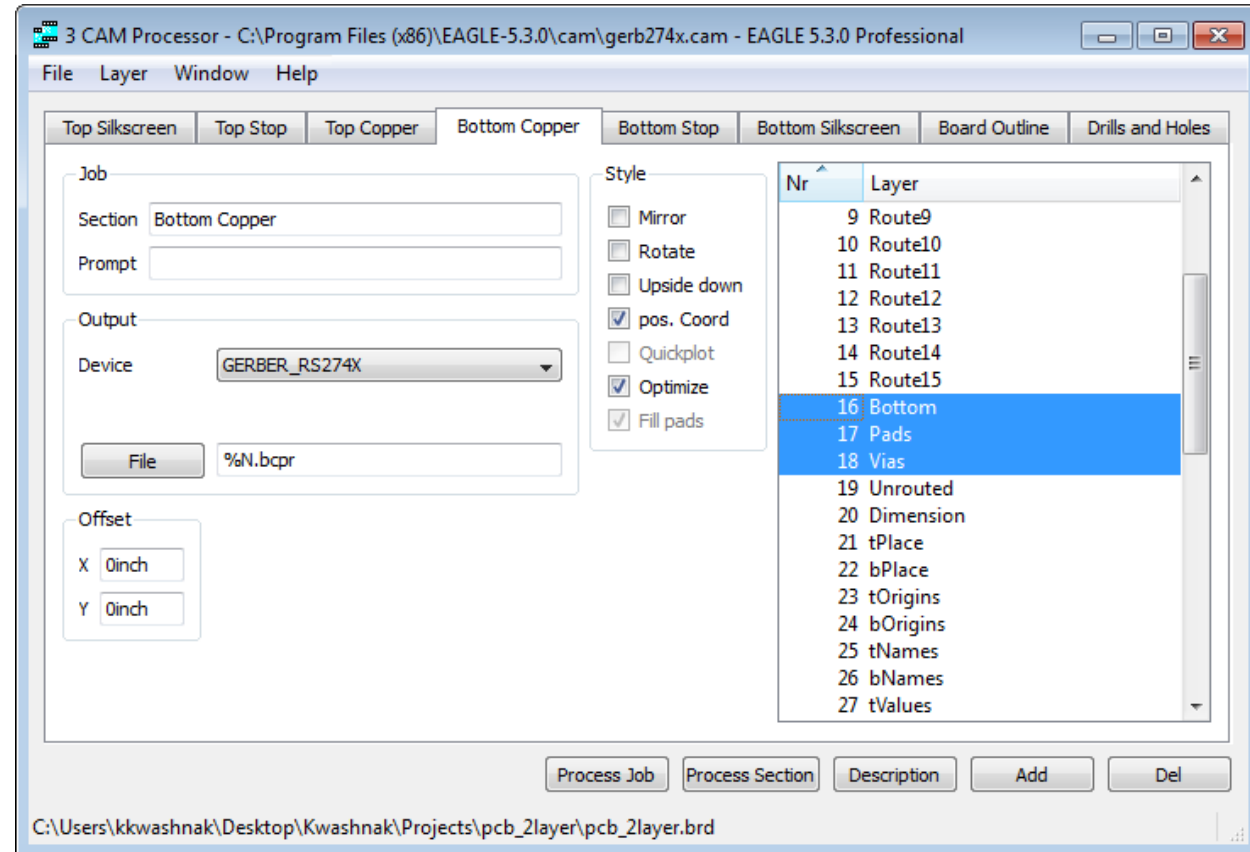
- ULPs
 - drillcfg.ulp
 - Configures drill holes
- CAM Processor
 - excellon.cam
 - Generates drill data
 - gerb274x.cam
 - Layers information



output = .tcpr

Two-Layer PCB Design - Step 15: Create Fabrication Files (cont.)

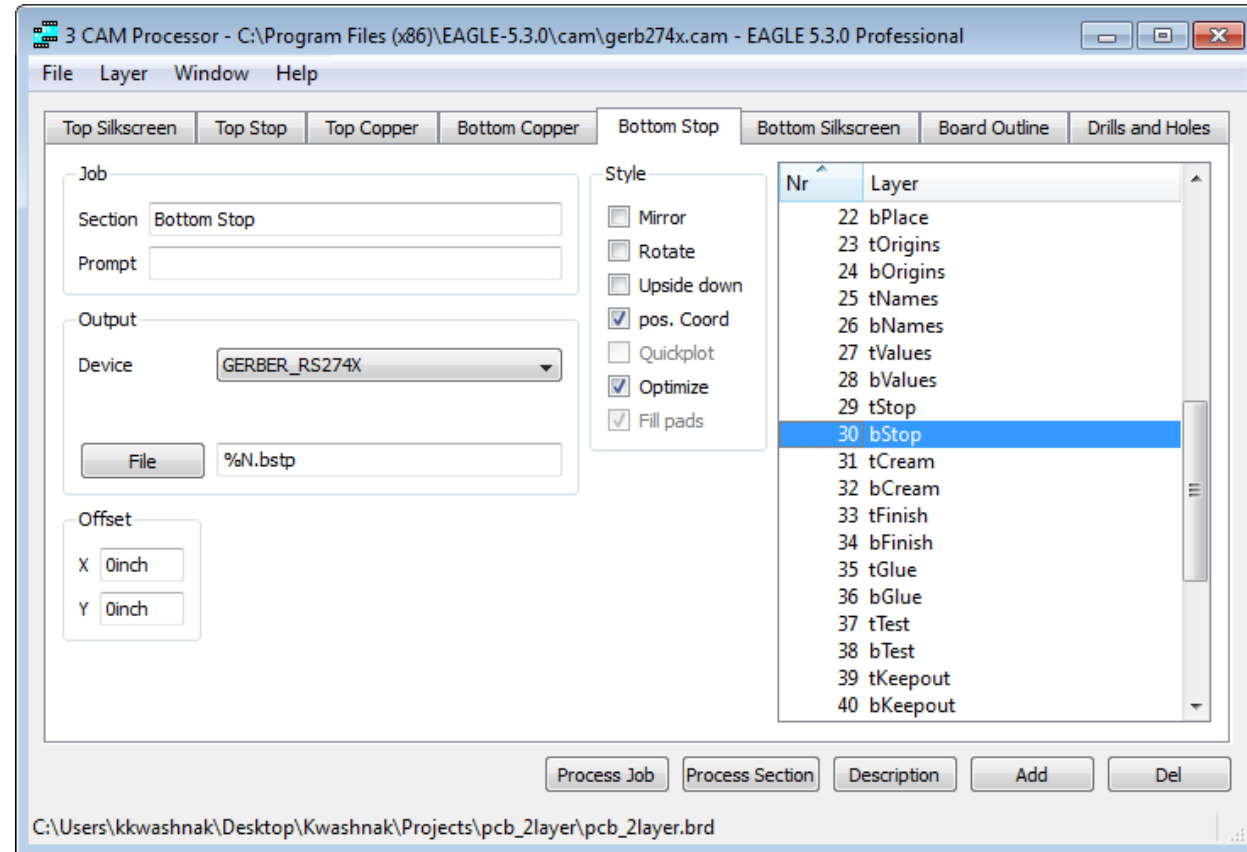
- ULPs
 - drillcfg.ulp
 - Configures drill holes
- CAM Processor
 - excellon.cam
 - Generates drill data
 - gerb274x.cam
 - Layers information



output = .bcpr

Two-Layer PCB Design - Step 15: Create Fabrication Files (cont.)

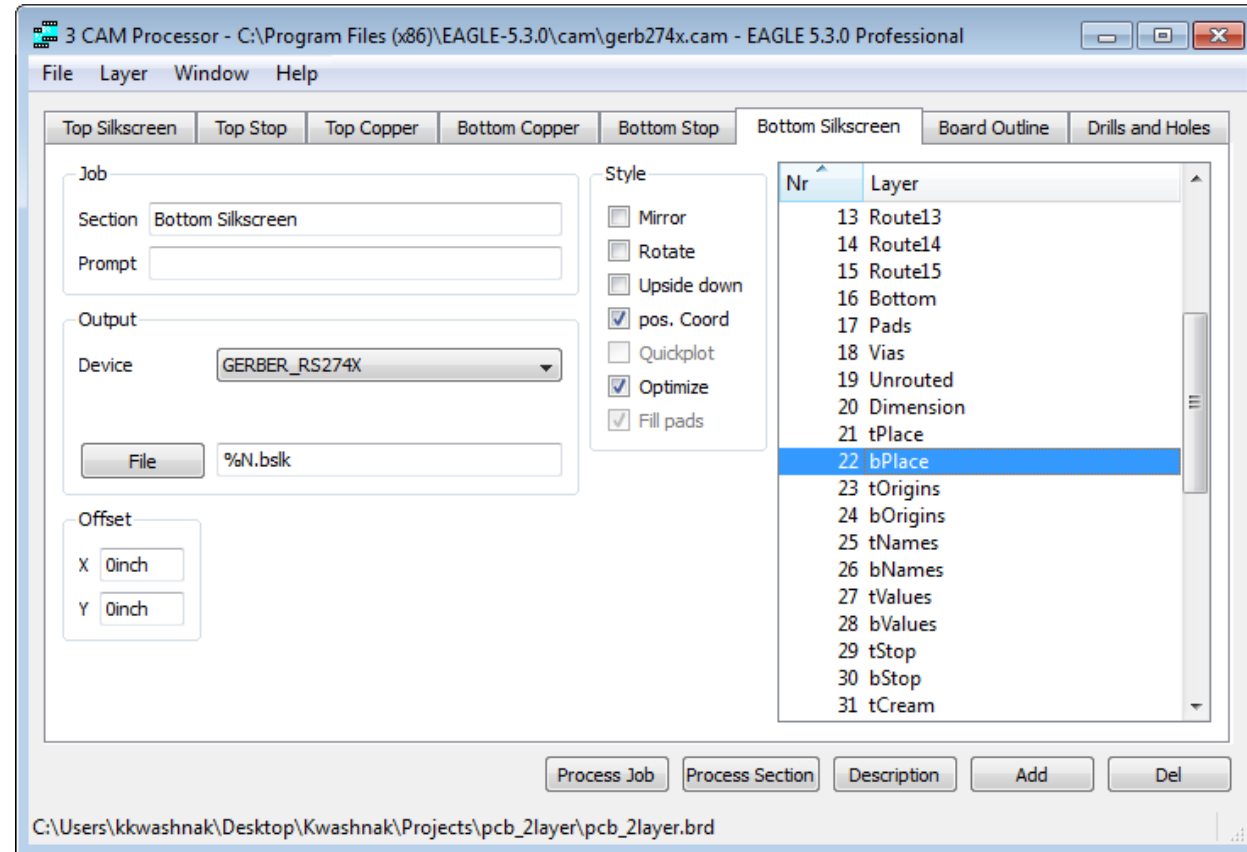
- ULPs
 - drillcfg.ulp
 - Configures drill holes
- CAM Processor
 - excellon.cam
 - Generates drill data
 - gerb274x.cam
 - Layers information



output = .bstp

Two-Layer PCB Design - Step 15: Create Fabrication Files (cont.)

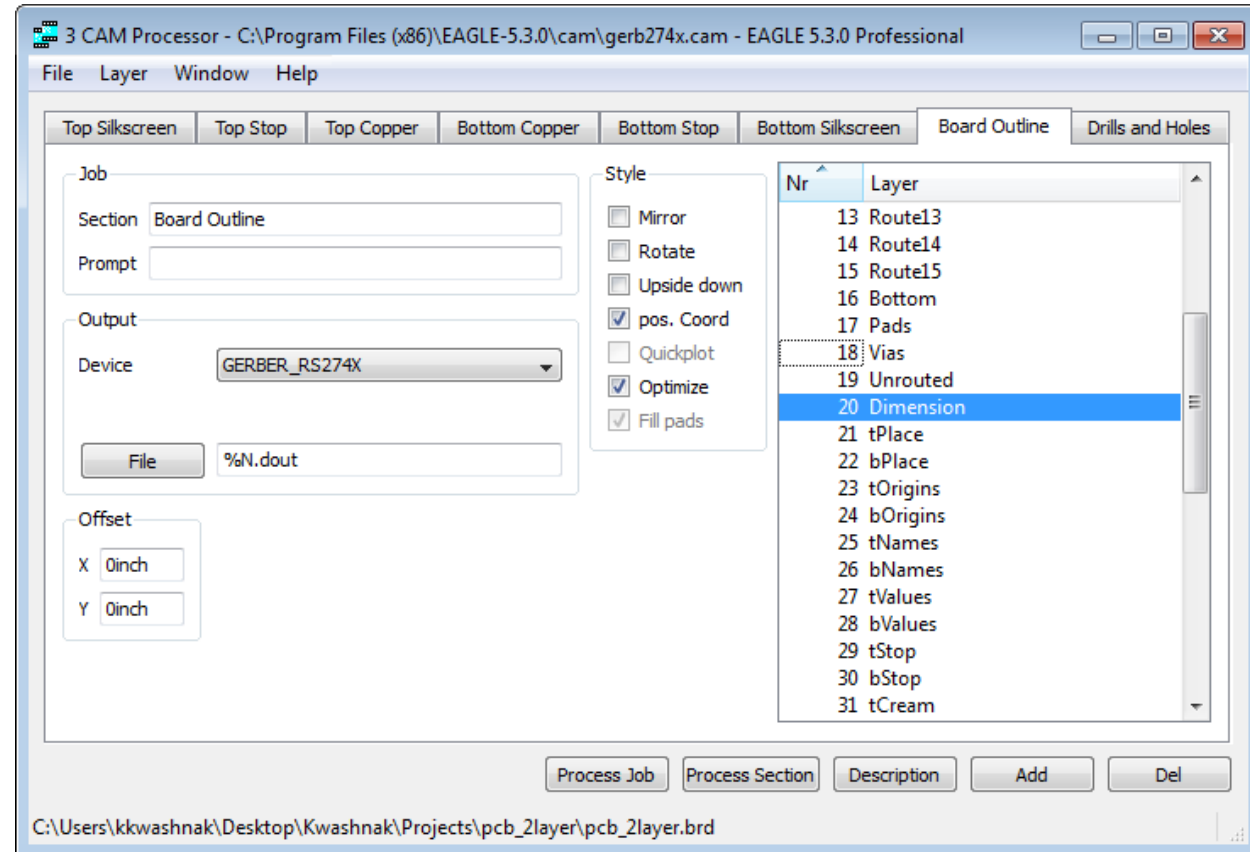
- ULPs
 - drillcfg.ulp
 - Configures drill holes
- CAM Processor
 - excellon.cam
 - Generates drill data
 - gerb274x.cam
 - Layers information



output = .bslk

Two-Layer PCB Design - Step 15: Create Fabrication Files (cont.)

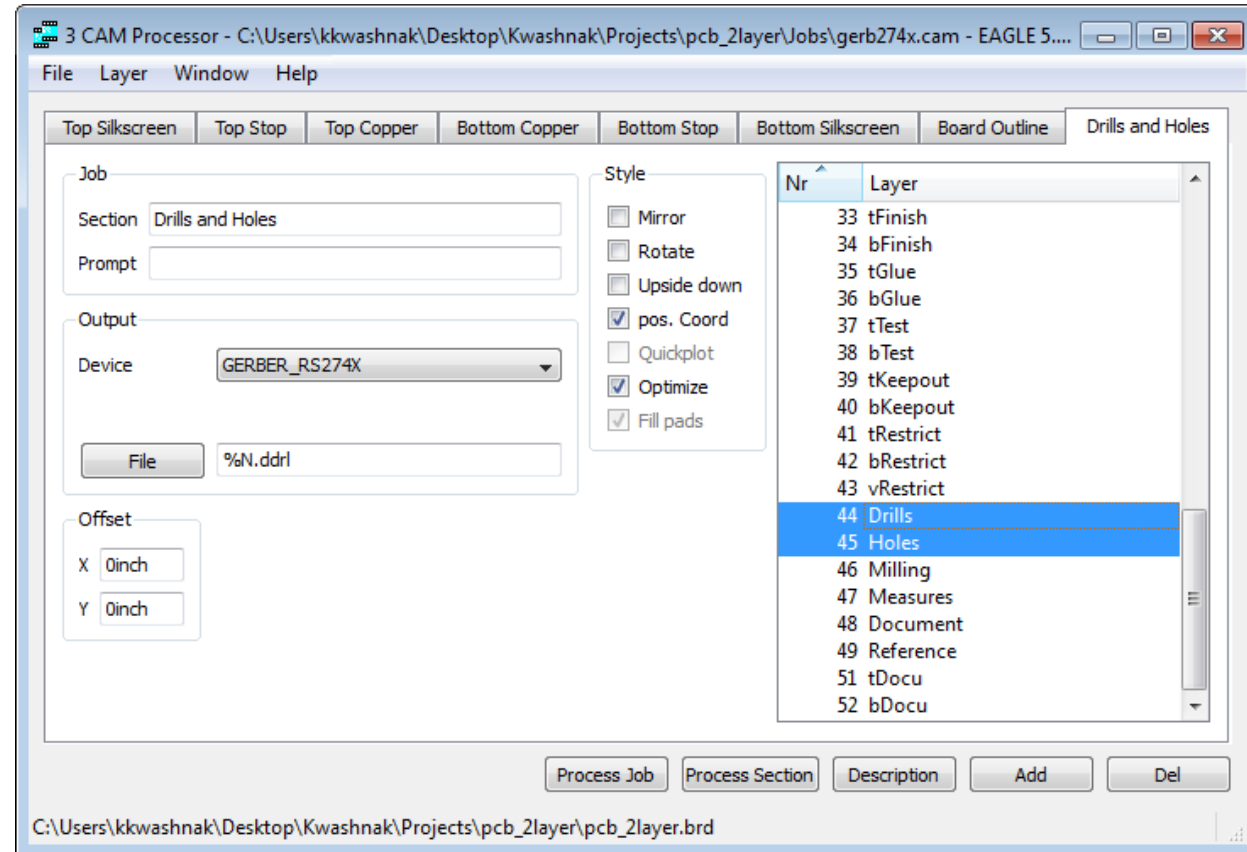
- ULPs
 - drillcfg.ulp
 - Configures drill holes
- CAM Processor
 - excellon.cam
 - Generates drill data
 - gerb274x.cam
 - Layers information



output = .dout

Two-Layer PCB Design - Step 15: Create Fabrication Files (cont.)

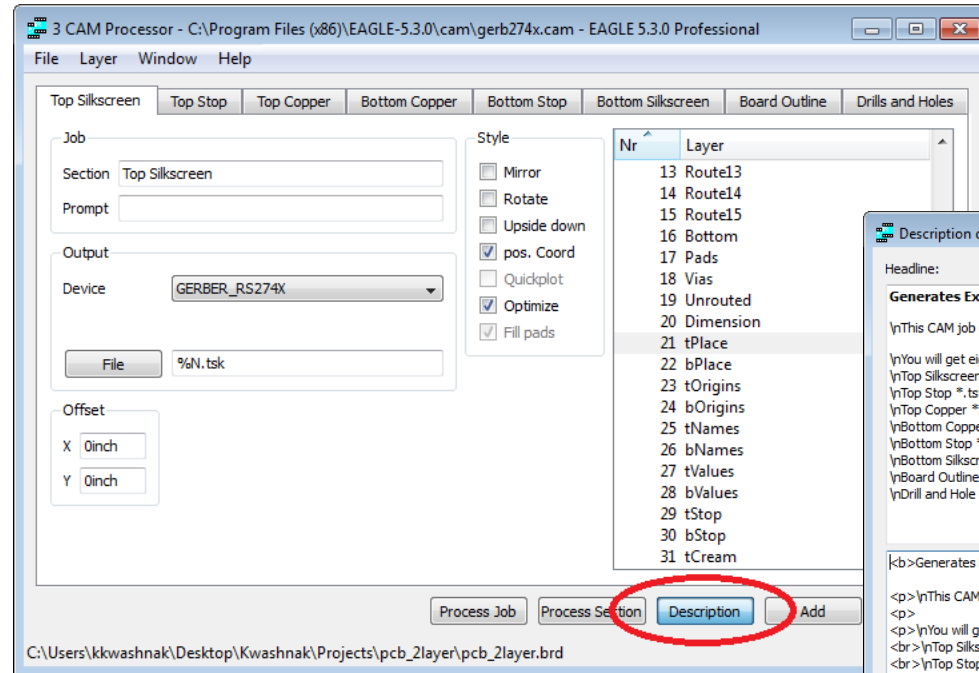
- ULPs
 - drillcfg.ulp
 - Configures drill holes
- CAM Processor
 - excellon.cam
 - Generates drill data
 - gerb274x.cam
 - Layers information



output = .ddrl

Two-Layer PCB Design - Step 15: Create Fabrication Files (cont.)

- ULPs
 - drillcfg.ulp
 - Configures drill holes
- CAM Processor
 - excellon.cam
 - Generates drill data
 - gerb274x.cam
 - Layers information



Two-Layer PCB Design - Step 16: Formulate Instructions

- Contact Information
- Software Used
- Tracing History
- Requirements
- Board Information
- Fabrication File Associations
- Description of Graphics Files

Author	Ken Kwashnak
Author Email	***@***.***
Author Phone	(***)***-****
Date	September 23, 2020
Board Name	Demo Board (pcb_2layer)
Board Version	1.0 (baseline)
Board Dimension	1.5" x 1.5" x 0.063"
Board Material	FR4
Copper Weight	1 oz
Lead Free	Yes
Soldermask	Both Sides
Soldermask Color	Green
Silkscreen	Both Sides
Silkscreen Color	White

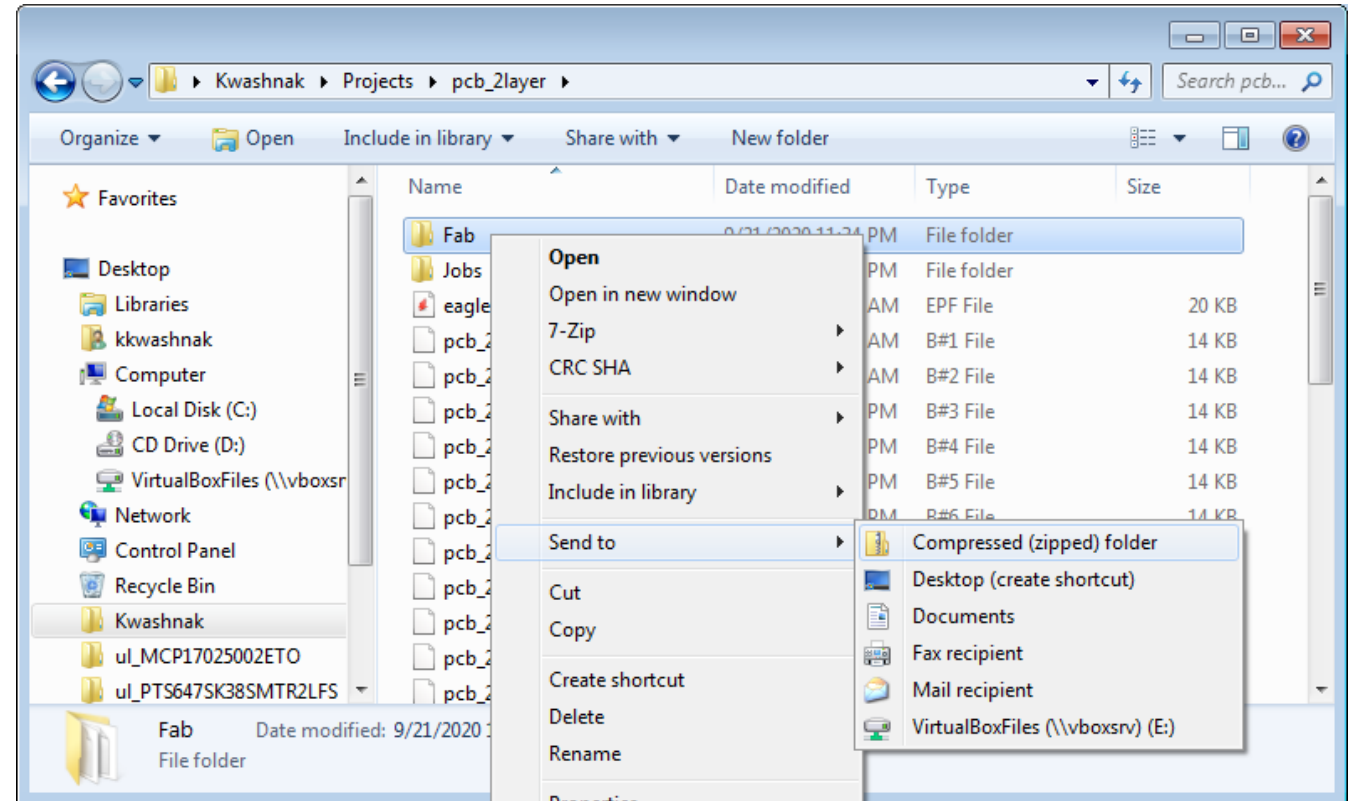
The attached fabrication files were processed from EAGLE v5.3.0:

- pcb_2layer.drl (Drill List)
- pcb_2layer.drd (excellon.cam, Drill Location Information)
- pcb_2layer.dri (excellon.cam, Drill Location Information)
- pcb_2layer.tslk (Gerber274x.cam, Top Silkscreen)
- pcb_2layer.tstp (Gerber274x.cam, Top Stop)
- pcb_2layer.tcpr (Gerber274x.cam, Top Copper)
- pcb_2layer.bcpr (Gerber274x.cam, Bottom Copper)
- pcb_2layer.bstp (Gerber274x.cam, Bottom Stop)
- pcb_2layer.bslk (Gerber274x.cam, Bottom Silkscreen)
- pcb_2layer.dout (Gerber274x.cam, Board Outline)
- pcb_2layer.ddr1 (Gerber274x.cam, Drills and Holes)
- pcb_2layer.gpi (Gerber274x.cam, Photoplotter)

Additional Notes:
- Plated Through Holes, Sized for No 4 Holes, Quantity 4

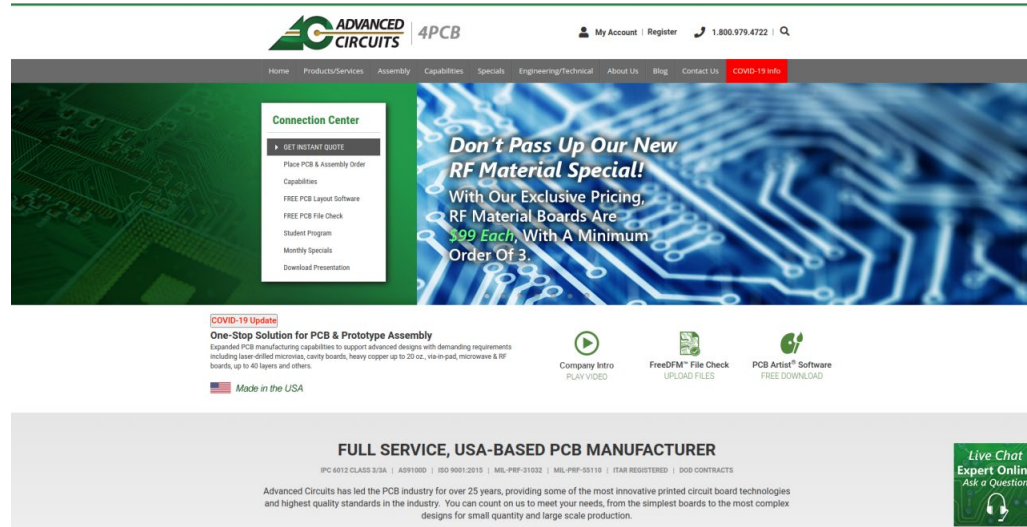
Two-Layer PCB Design - Step 17: Package Files

- Compress to a single folder
- Rename with tracing/
version control methodology
- Packaging may vary,
depending on the
manufacturer

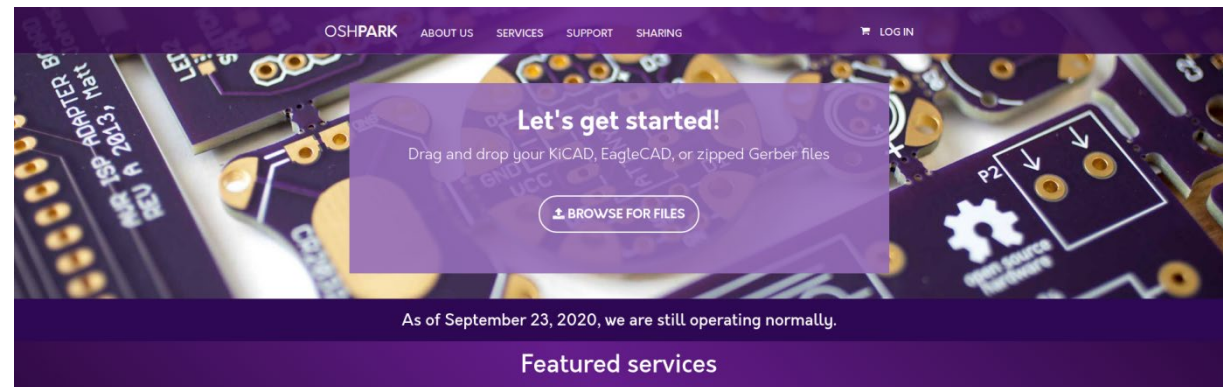


Two-Layer PCB Design - Step 18: Send to Manufacturer

- Read manufacturer license agreements before sending files
- Quote Auto-Gens may be fast but might not interpret your files correctly
- Call and talk to a rep in person to iron out details if you have questions or need clarifications



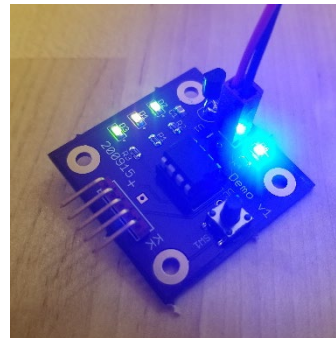
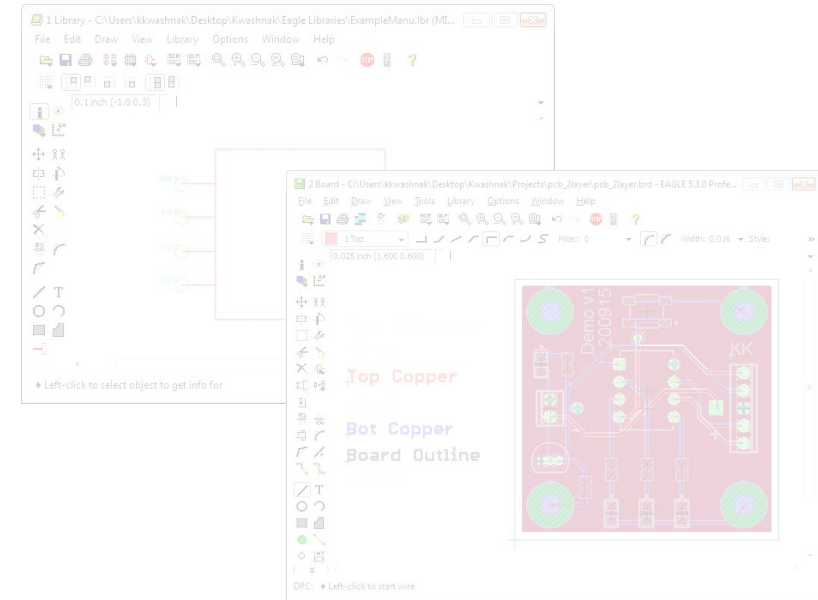
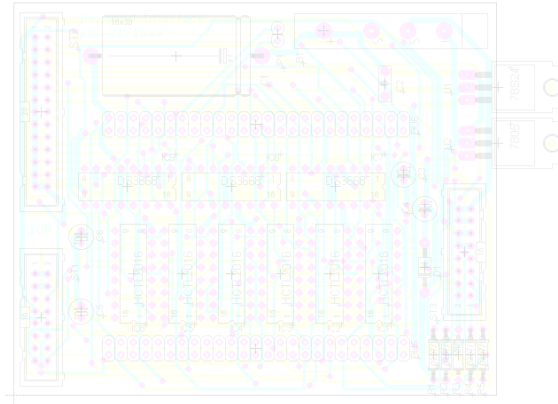
The screenshot shows the homepage of Advanced Circuits. The header includes the company logo, navigation links (Home, Products/Services, Assembly, Capabilities, Specials, Engineering/Technical, About Us, Blog, Contact Us), and a COVID-19 update link. A main banner features a blue circuit board background with the text: "Don't Pass Up Our New RF Material Special! With Our Exclusive Pricing, RF Material Boards Are \$99 Each, With A Minimum Order Of 3." Below the banner is a "Connection Center" sidebar with links like "GET INSTANT QUOTE", "Place PCB & Assembly Order", and "Capabilities". A "COVID-19 Update" section highlights "One-Stop Solution for PCB & Prototype Assembly". There are also icons for "Company Intro", "FreeDFM File Check", and "PCB Artist Software". The footer lists certifications and a "Live Chat Expert Online" button.



The screenshot shows the homepage of Oshpark. The header includes the company name and navigation links (ABOUT US, SERVICES, SUPPORT, SHARING, LOGIN). The main content area features a purple background with a circuit board image and a central call-to-action: "Let's get started! Drag and drop your KICAD, EagleCAD, or zipped Gerber files" with a "BROWSE FOR FILES" button. A banner at the bottom states: "As of September 23, 2020, we are still operating normally." Below this is a section for "Featured services".

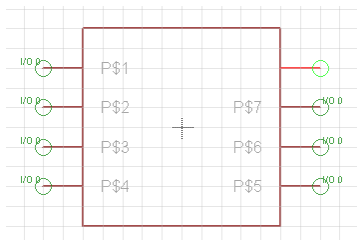
Agenda

- Introduction
- Setup
- Creating a Component (Device)
- Two-Layer PCB Design
- Discussion

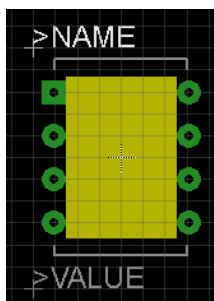


Discussion

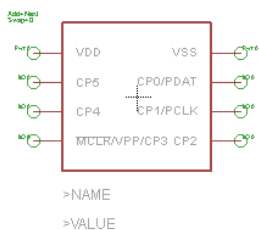
Symbol



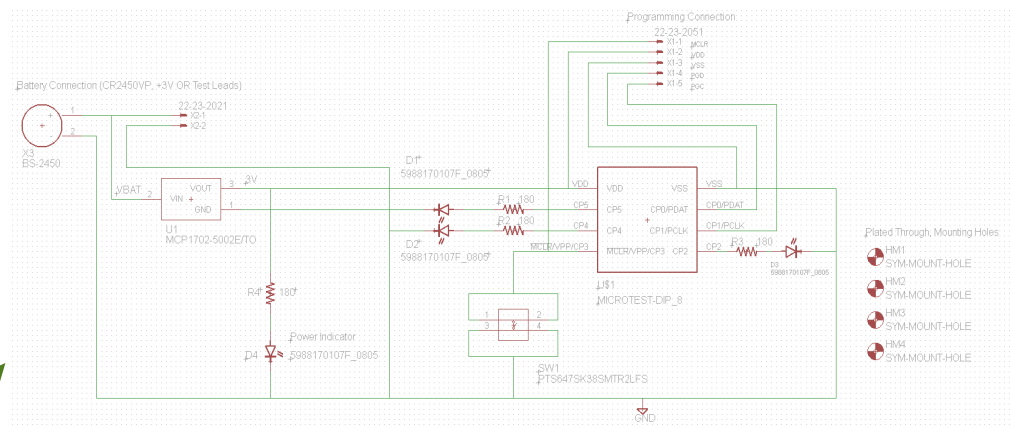
Package



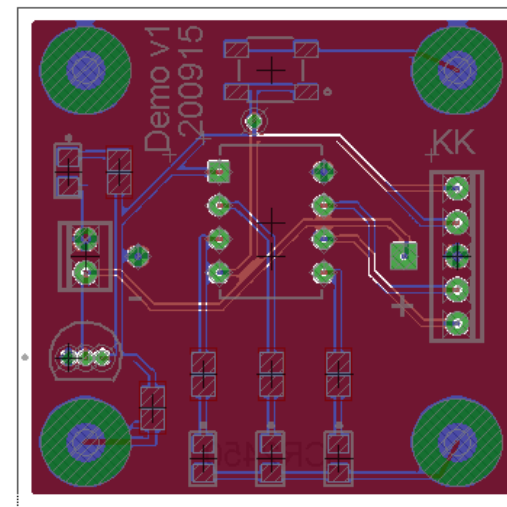
Device



Schematic



Board

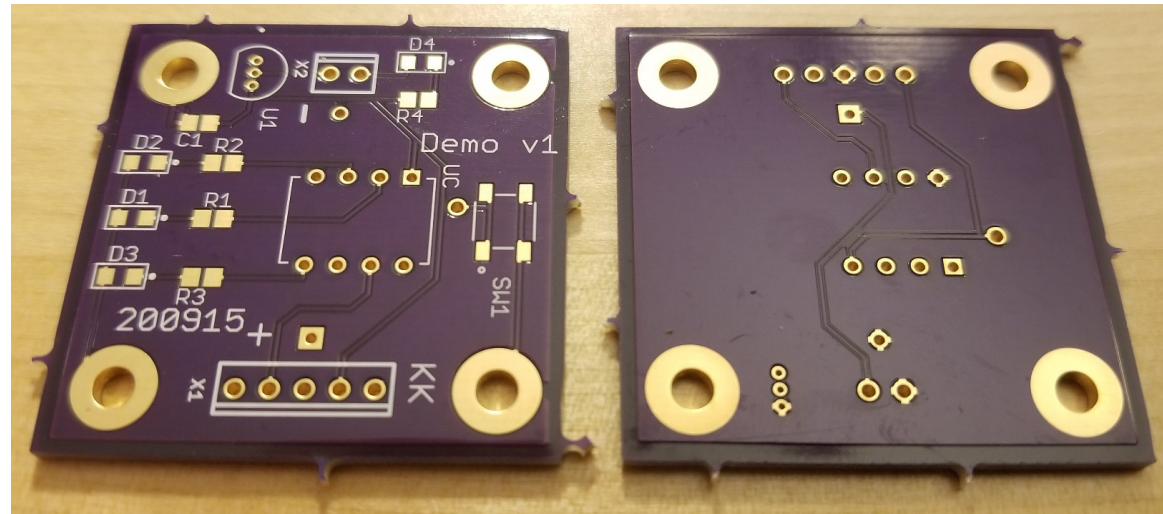
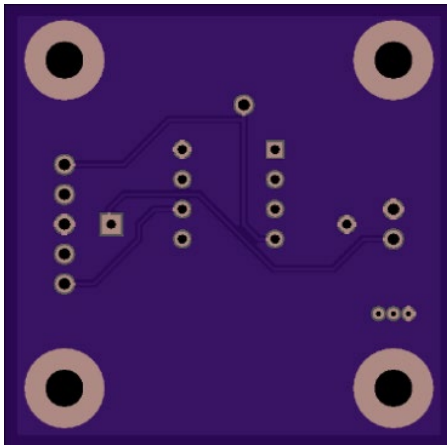
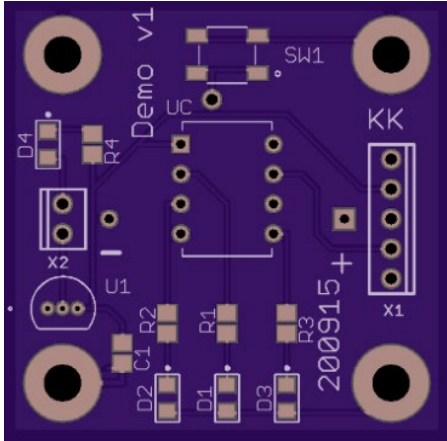


- Top Silkscreen
- tStop
- Top Copper
- bStop
- Bot Copper
- Board Outline
- Drills



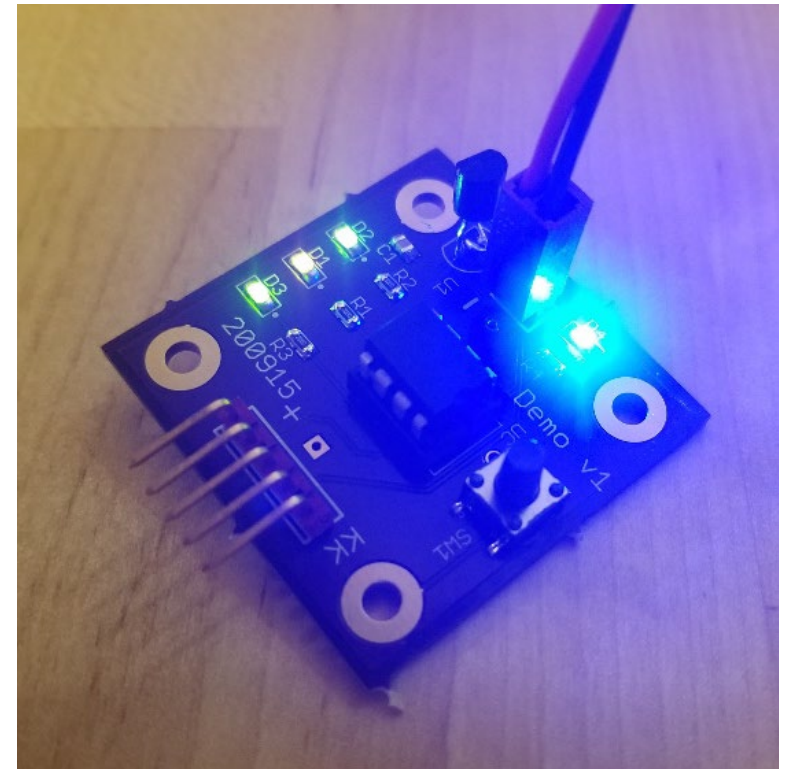
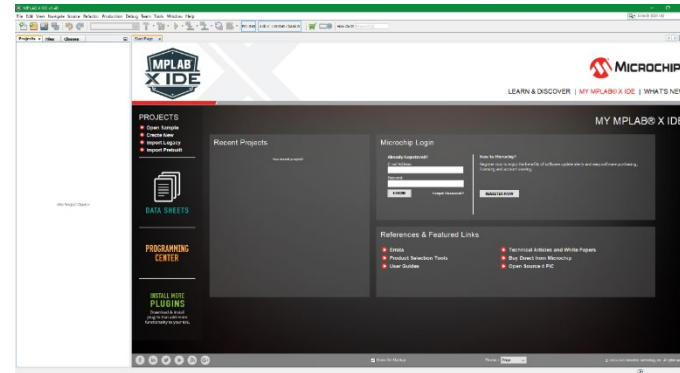
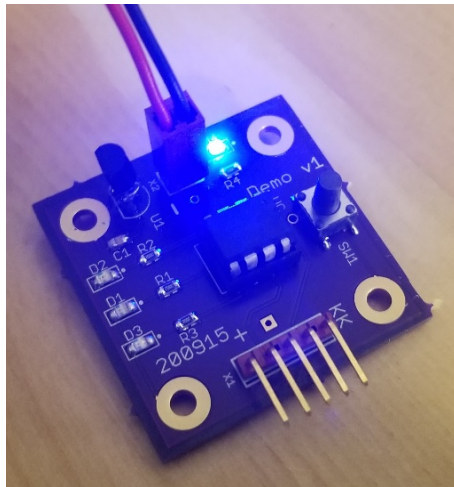
Discussion

- Oshpark fabricated board
- Drag and dropped my project into quoting system (did not create CAM or Gerber files)
- About a week turnaround time
- Fairly inexpensive
- Limited onboard styles
- No live reconfiguration tools



Discussion

- Utilized readily available components to populate board
 - Tested power - checked voltages and connections
 - Used MPLAB X, XC8 compiler to program microcontroller
 - Tested LED functionality
- Board functions as designed, with substitute parts!



Appendix A - Microcontroller Code

```
1. /* Author:          Ken Kwashnak
2.    Contact (e):     ***@***.***
3.    Contact (p):    (***)***_****
4.    Date:           October 8, 2020
5.    Platform:       Program intended for PIC12(L)F1501 for testing Demo v1.0 PCB functionality.
6.    Function:       Upon power on, individual LEDs illuminate. If switch is pressed, LEDs turn off.
7. */
8. // define crystal frequency
9. #define _XTAL_FREQ 16000000
10. #include <xc.h>
11. // Device Configuration, pg 38-39 of Microchip DS40001615C
12. // In order for the device to function properly, all registers must be configured.
13. // Clock settings
14. #pragma config CLKOUTEN = 1
15. // Brown-Out Reset
16. #pragma config BOREN = 00
17. // Code Protection
18. #pragma config CP = 1
19. // MCLR Pin Function
20. // since LVP is enabled, 1, this bit is ignored
21. #pragma config MCLRE = 0
22. // Power-Up Timer
23. #pragma config PWRTE = 1
24. // Watchdog timer
25. #pragma config WDTE = 00
26. // Oscillator settings
27. // using internal oscillator INTOSC
28. #pragma config FOSC = 00
29. // Low Voltage Programming
30. // based off of the voltage supplied to uC
31. #pragma config LVP = 1
32. // Low-Power Brown-out Reset
33. #pragma config LPBOR = 1
34. // Brown-out Reset Voltage
35. #pragma config BORV = 1
36. // Stack Over/Underflow Reset
37. #pragma config STVREN = 0
38. // Flash Memory Self-Write
39. #pragma config WRT = 11
40. void init(){
41. // I/O, PORTA Settings
42. // No alternate pin functions
43. // RA2, RA4, RA5 = Output = LEDs
44. // RA3 = Input = Push Button
45. // Direction Control, 1 input, 0 output
46. TRISA = 0x0B; // Binary: 0000 1011
47. // No Latch Register Definitions
48. // Analog Select Register
49. // Digital only
50. ANSELA = 0;
```

Appendix A - Microcontroller Code (cont.)

```
51. // Weak Pull-Up
52. // grounds input push button with switch closure, prevents floating
53. // input will read a high state, until button pressed
54. // no debouncing method or circuitry, not necessary
55. // Clearing register for individual pull-up use
56.  OPTION_REGbits.nWPUEN = 0;
57. // R3 Pull-up
58.  WPUA = 0x08; // Binary: 0000 1000
59. }
60. void main(void){
61. // Frequency Configuration
62.  OSCCONbits.IRCF = 0xF; // 1111 = 16MHz
63. // Internal Clock Configuration
64.  OSCCONbits.SCS = 3;
65. // Initializes device, as per function above
66.  init();
67. // Infinite Loop, Stay in State
68. // PORTAbits = reads state
69. // LATA = write state
70. // __delay_ms( time in milliseconds ); note, not best if you have interrupt service routines, ISRs
71. // the delay assists with the microcontroller performing the selected instruction
72. // ensures there's enough time to execute the next statement
73. // the loop essentially reads state of switch, if value is high, then write ON values to LEDs
74. // once the switch is pressed, input state goes low, and LEDs turn off

75. while(1){
76.   if(PORTAbits.RA3){
77.     LATA = 0b000100; // RA2
78.     __delay_ms(100);
79.     LATA = 0b010000; // RA4
80.     __delay_ms(100);
81.     LATA = 0b100000; // RA5
82.     __delay_ms(100);
83.   }else{
84.     LATA = 0b110100;
85.   }
86. }
87. }
```

Appendix B - Sample Library Device HTML Description

Headline: MICROTTEST-DIP_8

Author: Ken Kwashnak
Contact: ***@***.***
Date: August 20, 2020

This is a sample description file for a Library Device component.

1 Testing Parameters

Sample Text

- A: This is an indented line item. This is **BOLD** text.
- B: This is an indented line item. This is *ITALICIZED* text.
- C: This is an indented line item. This is UNDERLINED text.

o This is a double indented line item. Here is a combination of ***bold and italicized*** text.
o Sample Text!

2 List of Components

Table Header	
Item	Description
1	Sample Description 1
2	Sample Description 2

```
<!DOCTYPE html>
<html>
<body>
<title> MICROTTEST-DIP_8 </title>
<center><b>Author</b>: Ken Kwashnak
<br>
<b>Contact</b>: ***@***.***
<br>
<b>Date</b>: August 20, 2020 </center>

<p> <center> <i> This is a sample description file for a Library Device component. </i> </center> </p>

<p>
<h1> 1 Testing Parameters </h1>
Sample Text
<ul> <li>A: This is an indented line item. This is <b>BOLD</b> text. </ul>
<ul> <li>B: This is an indented line item. This is <i>ITALICIZED</i> text.</ul>
<ul> <li>C: This is an indented line item. This is <u>UNDERLINED</u> text.</ul>
<ul><ul> <li>This is a double indented line item. Here is a combination of <b><i>BOLD and ITALICIZED</i></b> text. </ul></ul>
<ul><ul> <li>Sample<sub>3</sub> Text<sup>1</sup> </ul></ul>
</p>
<hr><h1>2 List of Components </h1> </hr>
<table border=1 cellpadding="4" cellspacing="0" bgcolor="#ffffff" width="200" align="center">
<thead>
<tr>
<th colspan="2" style="color:white" bgcolor=black> Table Header</th>
</tr>
</thead>
<tbody>
<tr>
<td> <center>Item</center></td>
<td><center>Description</center></td>
</tr>
<tr>
<td> <center>1</center></td>
<td><center>Sample Description 1</center></td>
</tr>
<tr>
<td> <center>2</center></td>
<td><center>Sample Description 2</center></td>
</tr>
</tbody>
</table>
<!-- This is a comment -->
</body>
</html>
```

```
<!DOCTYPE html>
<html>
<body>
<title> MICROTTEST-DIP_8 </title>
<center><b>Author</b>: Ken Kwashnak
<br>
<b>Contact</b>: ***@***.***
<br>
<b>Date</b>: August 20, 2020 </center>

<p> <center> <i> This is a sample description file for a Library Device component. </i> </center> </p>

<p>
<h1> 1 Testing Parameters </h1>
Sample Text
<ul> <li>A: This is an indented line item. This is <b>BOLD</b> text. </ul>
<ul> <li>B: This is an indented line item. This is <i>ITALICIZED</i> text.</ul>
<ul> <li>C: This is an indented line item. This is <u>UNDERLINED</u> text.</ul>
<ul><ul> <li>This is a double indented line item. Here is a combination of <b><i>BOLD and ITALICIZED</i></b></i> text. </ul></ul>
<ul><ul> <li>Sample<sub>3</sub> Text<sup>1</sup> </ul></ul>
</p>
<hr><h1>2 List of Components </h1> </hr>
<table border=1 cellpadding="4" cellspacing="0" bgcolor="#ffffff" width="200" align="center">
<thead>
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<th colspan="2" style="color:white" bgcolor=black> Table Header</th>
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<td> <center>Item</center></td>
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<td> <center>1</center></td>
<td><center>Sample Description 1</center></td>
</tr>
<tr>
<td> <center>2</center></td>
<td><center>Sample Description 2</center></td>
</tr>
</tbody>
</table>
<!-- This is a comment -->
</body>
</html>
```

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