# A Basic Introduction for Designing a PCB with EAGLE eCAD/CAM Software

Kenneth M. Kwashnak Applied Physics Experimentalist and Researcher SURVICE Engineering Company CCDC Army Research Laboratory

October 28, 2020





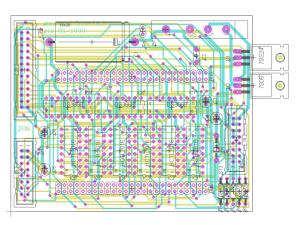
Defense Systems Information Analysis Center DSIAC is a DoD Information Analysis Center (IAC) sponsored by the Defense Technical Information Center (DTIC), with policy oversight provided by the Office of the Under Secretary of Defense (OUSD) for Research and Engineering (R&E). DSIAC is operated by the SURVICE Engineering Company.

Distribution A; Approved for Public Release; Distribution Unlimited



# Agenda

• Introduction

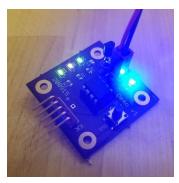


• Setup

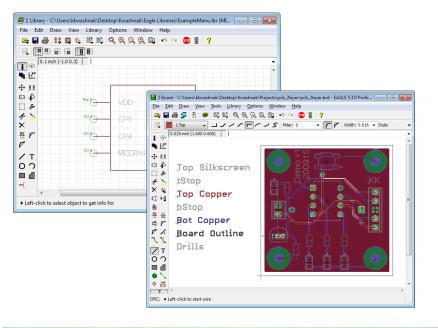
• Creating a Component (Device)

Two-Layer PCB Design

• Discussion



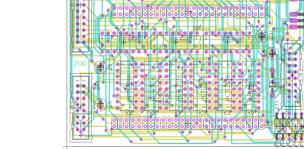






# Agenda

#### Introduction



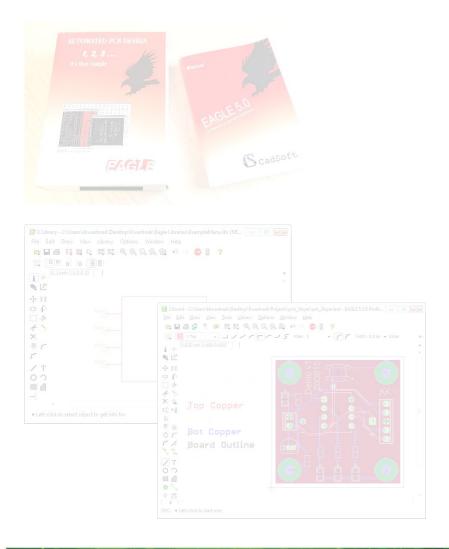
• Setup

• Creating a Component (Device)

Two-Layer PCB Design

• Discussion



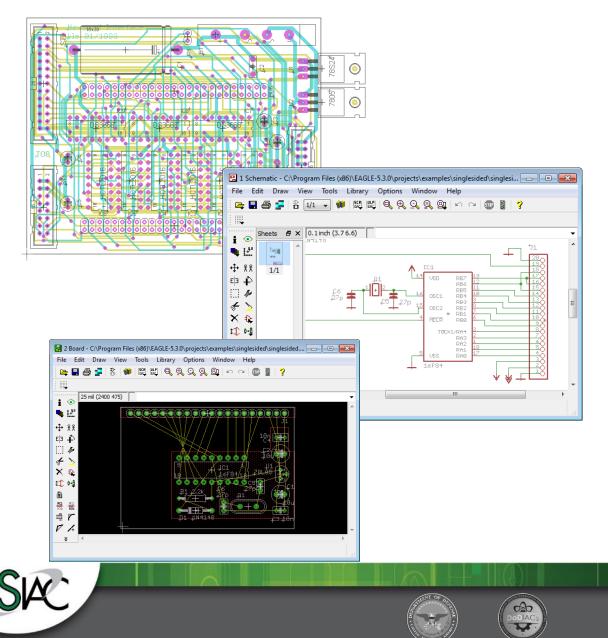


DODIAC

#### **Introduction - Overview**

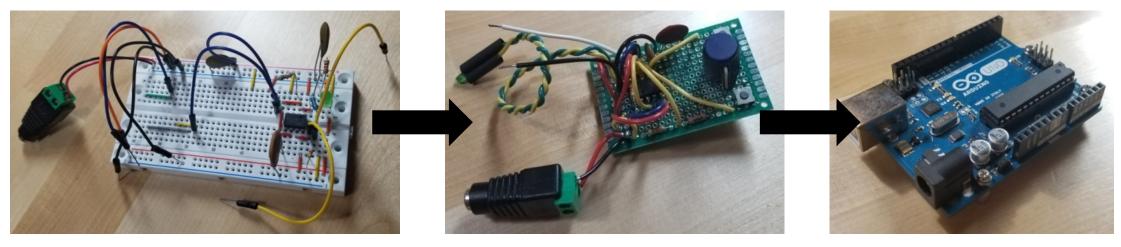
The Easily Applicable Graphical Layout Editor (EAGLE) is an electrical computeraided design (eCAD) and manufacturing (CAM) software. EAGLE supports the designer in transitioning prototype hardware to a more controlled precision design.

Printed circuit boards (PCBs) are electrical circuits etched on assorted laminates via conducting material, such as copper, that branch through various layers of insulating dielectric to form interconnected networks.



## **Introduction - Design Phases**

#### Typical Phases of Transitioning From a Prototype to a Professional Design



Bread Board

Perf Board



If the bread or perf board works, why make a PCB?

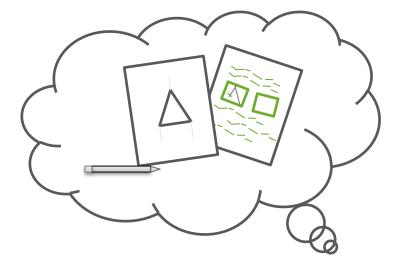
Quality. Assembly. Deterministic Behavior. Professional Look. Packaged. Requirements...





UNCLASSIFIED | Distribution Statement A: Approved for public release; distribution is unlimited.

## Introduction - eCAD





What do I need to create a PCB?

- All you will need is a pencil, paper, an idea, and a really clever manufacturer. However, that method will be costly, difficult to track, and time consuming.
- Not all manufacturers can guess what you need exactly, especially to conform to your requirements (they don't know what you don't write down, or they can guess and hope you like what they did).
- Essentially, you'll need an eCAD package that can captivate your idea and then generate the necessary manufacturing files. That's where the EAGLE eCAD software package comes into play.



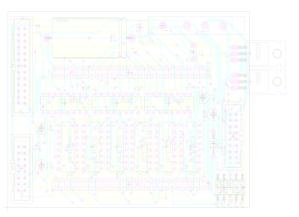


UNCLASSIFIED | Distribution Statement A: Approved for public release; distribution is unlimited.

# Agenda

Introduction

Setup



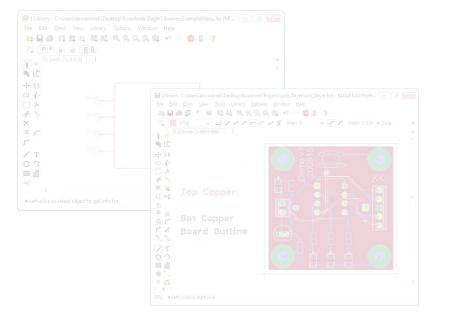
• Creating a Component (Device)

Two-Layer PCB Design

• Discussion







DODIAC

# **Setup - Circuit Programming and Testing**

Line	Description	Manufacturer	PN	Q	Cost Per Item [\$]	Total [\$]
1	No Clean Solder Wire 0.031" Tin/Cpr Core 66. LF	Kester (1)	24-9574-7618	1	55.39 <sup>1</sup>	55.39
2	Soldering Station, 35W	Aoyue (2)	936	1	42.75 <sup>2</sup>	42.75
3	No Clean Flux Paste Rosin	MG Chemicals (3)	8341-10ML	1	16.28 <sup>1</sup>	16.28
4	DC Linear Power Supply, Regulated, 0-30V, 0-5A	Korad (4)	KD3005D	1	85.00 <sup>3</sup>	85.00
5	Banana to Clip Cable (Red and Black Wires)	B&K Precision (5)	TL 5A	1	10.10 <sup>1</sup>	10.10
6	Multimeter, True RMS	Fluke (6)	117	1	219.99 <sup>1</sup>	219.99
7	Desolder Braid No Clean, Rosin, Non Activated, LF	Chemtronics (7)	60-5-5	1	6.55 <sup>1</sup>	6.55
8	Assorted Hook-Up Wire	Sparkfun (8)	PRT-11375	1	16.95 <sup>1</sup>	16.95
9	Cable Stripper and Cutter, 20 ~ 30 AWG	Hakko (9)	CSP-30-1	1	14.06 <sup>1</sup>	14.06
10	Tweezer Set	Wiha (10)	44593	1	207.96	207.96
11	Isopropyl, Cleaning Agent	MG Chemicals (11)	824-1L	1	16.75 <sup>1</sup>	16.75
12	Brush	MG Chemicals (12)	855-5	1	4.45 <sup>1</sup>	4.45
13	PICKit3	Microchip (13)	PG164130	1	25.00 <sup>4</sup>	25.00
14	PICKit3 Programming Cable	Digilent (14)	240-035	1	3.99 <sup>1</sup>	3.99
15	ESD Caliper	Wiha (15)	41105	1	74.56 <sup>1</sup>	74.56

1 - Data from Digikey on October 8, 2020

2 - Data from Aoyue3d on October 8, 2020

- 3 Data from SRA Soldering Equipment on October 8, 2020
- 4 Data from Amazon on October 8, 2020



A

## **Setup - PCB Components**

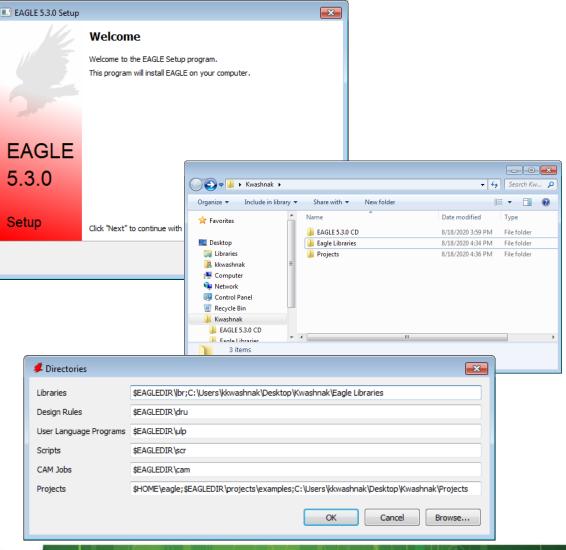
Line	Description	Manufacturer	PN	Q	Cost Per Item [\$] <sup>1</sup>	Total [\$]
1	Microcontroller, DIP8	Microchip (16)	PIC12LF1501	1	0.77000	0.77
2	IC DIP Socket 8POS	Adam Tech (17)	ICS-308-T	1	0.15000	0.15
3	Battery, CR2450, 3V	Energizer (18)	CR2450VP	1	1.19000	1.19
4	Battery Holder, Coin PC Pin	MPD (19)	BS-2450	1	1.09000	1.09
5	Regulator Linear 3V, TO92 -3	Microchip (20)	MCP1700-3002E/TO	1	0.37000	0.37
6	Green Smd LED	Dialight (21)	5988170107F	4	0.39000	1.56
7	Tactile Switch, NO	C&K (22)	PTS 647 SK38 SMTR2 LFS	1	0.13000	0.13
8	Res, 0805, 120?, 5%, 1/8W	Vishay Dale (23)	CRCW0805120RJNEA	4	0.10000	0.40
9	Cap, 0805, 0.1uF, 25V, X7R	KEMET (24)	C0805C104M3RACTU	1	0.10000	0.10
10	0.100" Header, 5 Pin, Prog	Molex (25)	22-23-2051	1	0.34000	0.34
11	0.100", Conn Housing, 5POS	Molex (26)	0022012057	1	0.23000	0.23
12	0.100" Header, 2 Pin, Batt	Molex (27)	22-23-2021	1	0.17000	0.17
13	0.100", Conn Housing, 2POS	Molex (28)	0022012027	1	0.11000	0.11
14	Conn 22-30AWG Crimp Tin	Molex (29)	0008650804	7	0.10000	0.70

1 - Price from Digikey as of September 18, 2020

DODIAC

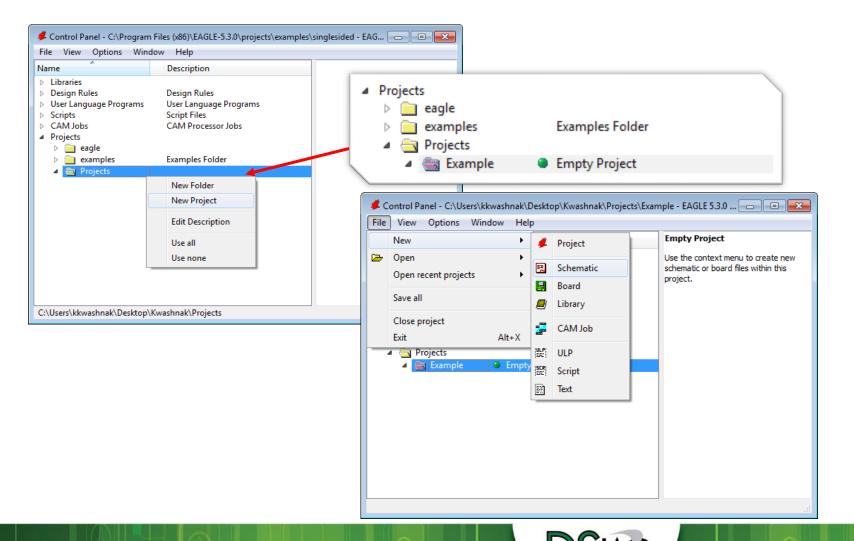
# **Setup - Computer**

- Using a laptop with Ubuntu 16.04 OS, run an isolated Windows 7 x 64 virtual OS on VirtualBox v5.1.38
- Install software
  - EAGLE v5.3.0
  - MPLAB X IDE v5.4.0 and XC8 Compiler v2.30
- In virtual OS, form a file structure to house design records
- Add pathways to EAGLE's directories





# Setup - Project



- Create a project
- Activate project
- Add file
  - Schematic
  - Board
  - Library
  - CAM job

a

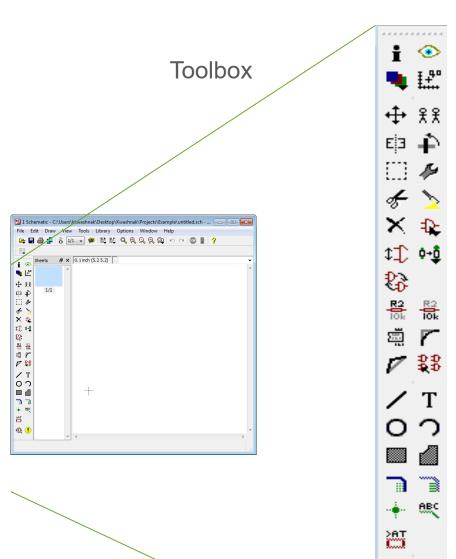
- ULP
- Script
- Text

# Setup - Software

#### **Graphical Conventions**

			Schematic Editor	
#	Name	#	Color	Comment
1	Nets	91	Dark Green	
2	Buses	92	Dark Purple	Consists of multiple Nets
3	Pins	93	Dark Green	
4	Symbols	94	Dark Red	
5	Names	95	Dark Grey	
6	Values	96	Dark Grey	
7	Info	97	Dark Grey	
8	Guide	98	Dark Yellow	

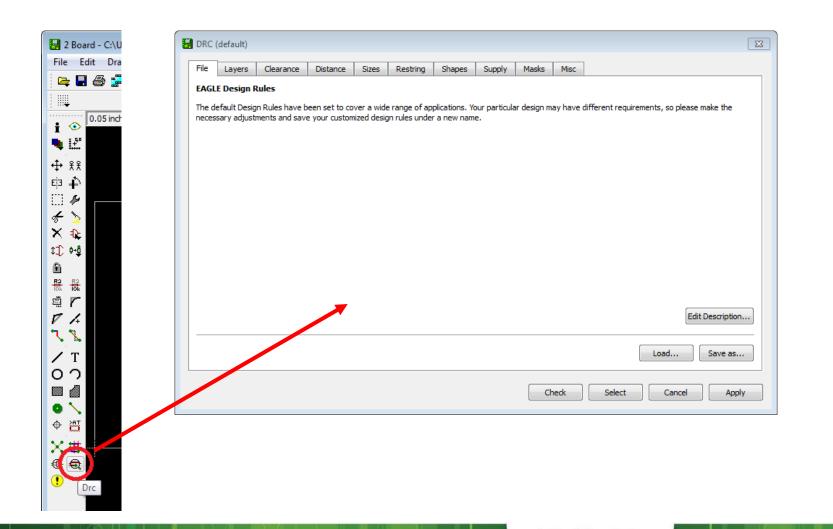
			Вс	oard Editor				
#	Layer Group	Name	#	Color Name		Color	Comment	Gerber
1	Top Silkscreen	tPlace	21	Light Grey				.tslk
2	Green Top	tStop	29	Black with Line			Keep Out Region	.tstp
3	Top Copper	Top, Pads, Vias	1, 17, 18	Red, Dark Green, Dark Green				.tcpr
4	Bottom Copper	Bottom, Pads, Vias	16, 17, 18	Blue, Dark Green, Dark Green				.bcpr
5	Green Bottom	bStop	30	Black with Line				.bstp
6	Bottom Silkscreen	bPlace	22	Dark Grey				.bslk
7	Board Outline	Dimension	20	Light Green				.dout
8	Drills, Holes	Drills, Holes	44, 45	Dark Grey, Dark Grey				.ddrl
9	Top Restriction Zone	tRestrict	41	Red with Dots				
10	Bottom Restriction Zone	bRestrict	42	Blue with Dots	/			
11	Origins, Top	tOrigins	23	Light Purple			Part Manipulation	
12	Origins, Bottom	bOrigins	24	Dark Purple			Part Manipulation	
13	Name, Top Component	tNames	25	Light Grey			Appears on silkscreen	
14	Name, Bottom Component	bNames	26	Dark Grey			Appears on silkscreen	
15	Document Notes, Top	tDocu	51	Light Yellow			PCB Physical View	
16	Document Notes, Bottom	bDocu	52	Dark Yellow			PCB Physical View	





Ð 🕑

#### **Setup - Design Manufacturing Requirements**



- Toolbar button
   <Drc>
- Set requirements for board layout
  - Layers
  - Clearance
  - Distance
  - Sizes
  - Restring
  - Shapes
  - Supply
  - Masks

CAD DODIAC

• Misc.

## Setup - DRC, Layers

	ers Clearance	Distance	Sizes	Restring	Shapes	Supply	Masks	Misc
1			Nr 1 0.03 16 0.03		Copper			Isolation
		ther <i>core</i> or <i>p</i>		aterial. <b>a*b</b> d	combines laye	ers a and b	with a <i>core</i>	e, while <b>a+b</b> does the same with <i>prepreg</i> .
	through vias are of redefined by writin	defined by wri g [t::b	_		d via from to		and from h	

- Layer stack-up.
- The setup field defines the custom text field to define board stack-up.
- (1\*16) => two-layer board.
- ((1\*2)+(15\*16)) = ?
   multilayered board.
- (2:1 + ((2\*3)+(14\*15))+15:16)
   => multilayered board
   with blind vias.

#### **Setup - DRC, Clearance**

le Layers Clearance	Distance	Sizes	Restring	Shapes	Supply	Masks	Misc			
						Differe	ent Signa	als		
			Wire	e						
	Wire	e 8mil					Pad			
	Pad	8mil			8mil				Via	
	Via	8mil			8mil				8mil	
							e Signals	5		
			Smo	8			Pad		Via	
	Smo	8mil			8mil				8mil	
inimum Clearance betwe the Same Signals check bet etting the values for the Sar	ween <i>Smd</i> and <i>V</i>	<i>ïa</i> does r	not apply to A		edk.					

- Minimum distance between objects in signal layers
- Specify according to Wire, Pad, Via, or Smd

A

#### **Setup - DRC, Distance**

🛃 DRC	(default)													<b>_</b> ×
File	Layers	Clearance	Distance	Sizes	Restring	Shapes	Supply	Masks	Misc					
		nce between a	Dri  objects in sign	ll/Hole al layers (		and any cop	per connect	ed to them	) and the	e board di	mensions	, and betwe	een drill hole:	5.
								d	heck	Se	ect	Cance		Apply

- Minimum distance between objects in signal layers, in addition to board dimensions and drill holes
- Specify according to copper or drill hole

A



#### Setup - DRC, Sizes

DRC (default)
File         Layers         Clearance         Distance         Sizes         Restring         Shapes         Supply         Masks         Misc
Minimum Width       10mil         Minimum Drill       24mil         Min. Micro Via       9.99mm         Min. Blind Via Ratio       0.5
Min. Micro Via applies to <i>blind</i> vias that are exactly one layer deep. Typical values are in the range 50100 micron. A value larger than Minimum Drill (e.g. the default value of 9.99mm) means there are no micro vias.
Min. Blind Via Ratio defines the minimum drill diameter d'a blind via must have if it goes through a layer of thickness t. Board manufacturers usually give this "aspect ratio" in the form 1:0.5, where 0.5 would be the value that has to be entered here.
Check Select Cancel Apply

Minimum width of any objects in the signal layers and drill holes

## **SETUP - DRC, Restring**

File Layers	Clearance	Distance	Sizes	Restrir	ng Shapes	Supply	Masks	Misc		
					Min			%	Max	Diamete
	-	Pa	ds	Тор	10mil		25		20mil	
		L		Inner	10mil		25		20mil	
				Bottom	10mil		25		20mil	
_		Via	<u>د</u>	Outer	8mil		25		20mil	
			2	Inner	8mil		25		20mil	
				1000			23		2011	
		Mie	cro Vias	Outer	4mil		25		20mil	
				Inner	4mil		25		20mil	
arger restring, if the <b>Diamet</b> o Micro Vias are	that value will be er option is check	e used in the o red the actual re exactly one	uter laye pad or vi e layer de	rs. ia diamete eep and h	er will be taken i	nto account	in the inne	r layers, too.	f an actual pad or via would n Drill value defined under .	

- Width of the copper ring that must remain after the Pad or Via has been drilled
- Specify per Pads, Vias, and Micro Vias

A

#### **SETUP - DRC, Shapes**

DRC (	(default)											
File	Layers	Clearance	Distance	Sizes	Restring	Shapes	Supply	Masks	Misc			
			Sn	nds		м	in			%		Мах
			/	Roun	dness	Omil		0			Omil	
		Y	₩ Pa	ds					s	паре		
				Тор		As in library						•
				Botto	m (	As in library						•
				First		Not special						•
				Elong	ation %	100		100			]	
Shap	es of pads a	and smds.										
								d	heck	Select	Cance	el Apply

 Geometry of Pads and Smds

DoDIACS



#### Setup - DRC, Masks

📕 DRC (default)										×
File Layers Clearance Distance	e Sizes	Restring	Shapes	Supply	Masks	Misc				
		I	Min			%			Max	
	Gap	20mil		50	)			100mi	il	
		Is	olate			Restring				
	Thermal [	10mil				1				
	Annulus	20mil								
×	Gener	ate thermals fo	r vias							
Supply symbols are generated for pads a										
If a <b>Restring</b> is deactivated for <b>Annulus</b> The <b>Gap</b> is defined in percent of the drill d				fully filled cir	de instead	d of a ring	<b>]</b> .			
The Thermal Isolate parameter will also										
NOTE: The actual shape of supply symbols				tput for pho	toplotters	that use	specific ther	mal/ann	ulus apertures!	
					C	heck	Select		Cancel	Apply

 Geometry of the Thermal and Annulus symbols used in the supply layers

DoDIAC

## Setup - DRC, Masks (cont.)

File	Layers	Clearance	Distance	Sizes	Restring	Shapes	Suppl	y Masks	Misc			
					M	ſin			%		Max	
			Stop	o 4mil				100		4mil		
			Crea	am Omil				0		 Omil		
			Limit	t Omil								
		<b>b</b>										
			<sup></sup>									
Mask	values are	e defined in per	cent of the sma	aller dime	nsion of smd	s, pads and v	/ias (lim	ited by <b>Min</b> a	nd Max).			
Stop	masks are <u>g</u>	generated for s	mds, pads and							 		
Stop	masks are <u>g</u>		mds, pads and							 		
Stop	masks are <u>g</u>	generated for s	mds, pads and							 		
Stop	masks are <u>g</u>	generated for s	mds, pads and									
5top	masks are <u>g</u>	generated for s	mds, pads and									
Stop	masks are <u>g</u>	generated for s	mds, pads and							 		

 Dimensions of the Solder Stop and Cream Masks

DoDIAC



#### Setup - DRC, Miscellaneous

File	Layers	Clearance	Distance	Sizes	Restring	Shapes	Supply	Masks	Misc				
C	heck grid												
C	heck angle												
V C	heck font												
√ C	heck restrict	t											
The C	<b>rid</b> chack w	orifies that all r	ade ende vi	ise and wi	res in signal l	avers are o	the curren	t orid			 		
		erifies that all p					n the curren	t grid.			 		
		erifies that all p reports signal					n the curren	t grid.			 		
							n the curren	t grid.			 		
							n the curren	t grid.			 		
							n the curren	t grid.			 		
							n the curren	t grid.					
							n the curren	t grid.					
							n the curren	t grid.					
							n the curren		heck	Select		Арр	

• Grid settings and Angle checks





# Agenda

Introduction

• Setup

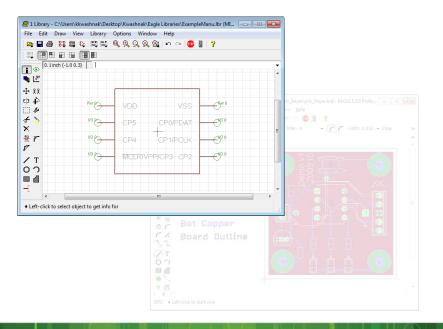
- Creating a Component (Device)

Two-Layer PCB Design

• Discussion









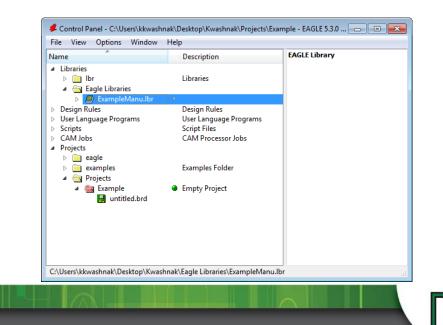


#### **Creating a Component (Device) - Overview**

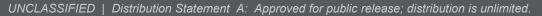
#### A component comprises three main elements in EAGLE:

- 1. Symbol (used in the Schematic Editor)
- 2. Package (used in Board Editor)
- 3. Device (stored in library file that the Schematic and Board Editor reference)

The device is stored in a library, which houses various devices, symbols, and packages.



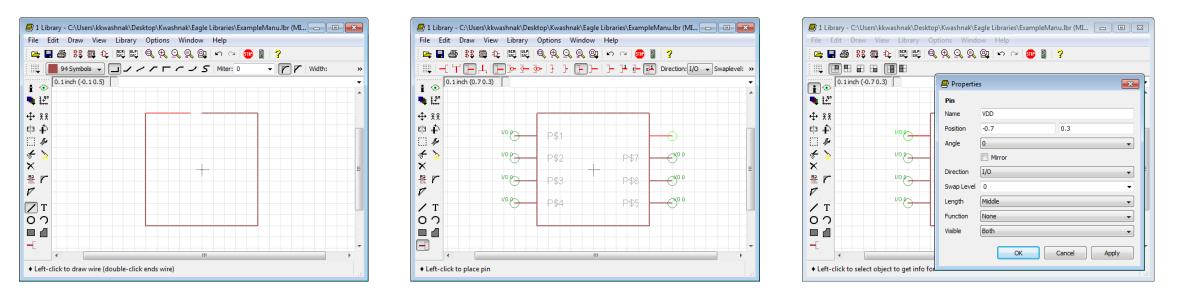
🧧 Edit	×
Package	
New:	
Dev Pac	Sym
OK	Cancel





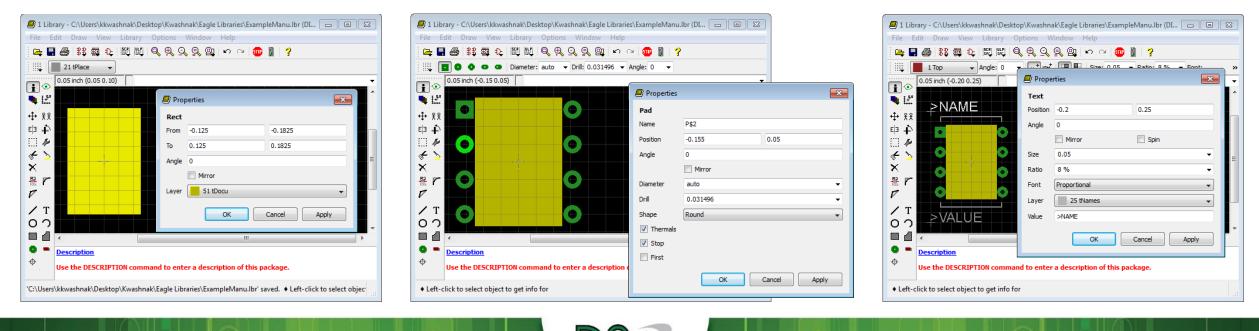
## **Creating a Component (Device) - Symbol**

- The symbol should be designed first and referenced from the datasheet.
- Two main conventions for symbols:
  - 1. Ordered looks exactly like the pinout of the device.
  - 2. Functional pins are associated to their respective type of signal.
- Draw the component outline, add pins, and define all pin properties.



## **Creating a Component (Device) - Package**

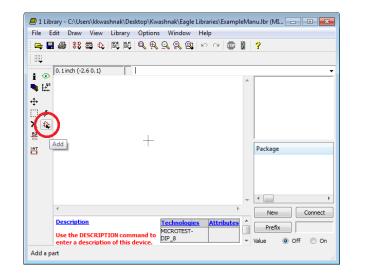
- The package will have multiple defined layers:
  - Silkscreen component outline and labels (29 tPlace, 22 bPlace, 25 tNames, 26 bNames)
  - Pin holes/drills (44 drills, 45 holes)
  - Restriction zones
  - Clearance areas
- Draw the component body outline, add pins, configure pin properties, add text, and outline info.

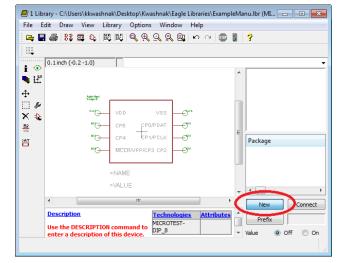


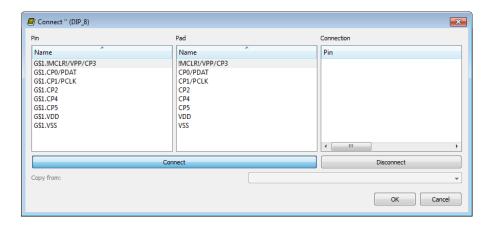


## **Creating a Component (Device) - Device**

- Compiles symbol and package data into one object
- Allows creation of part variations
- Adds descriptions (in HTML format)
- Adds/places symbol, creates a new package, and associates connections (pins to pads)



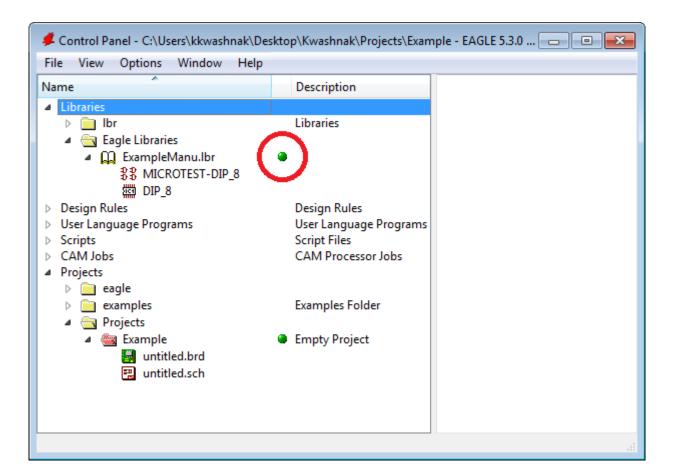








#### **Creating a Component (Device) - Activate Library**



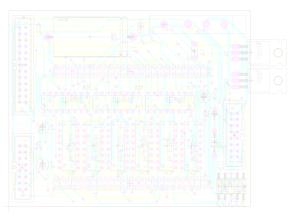


A

# Agenda

Introduction

• Setup



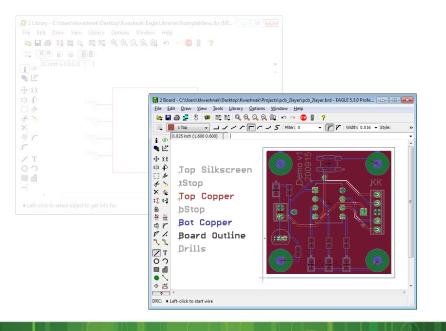
• Creating a Component (Device)

Two-Layer PCB Design

• Discussion



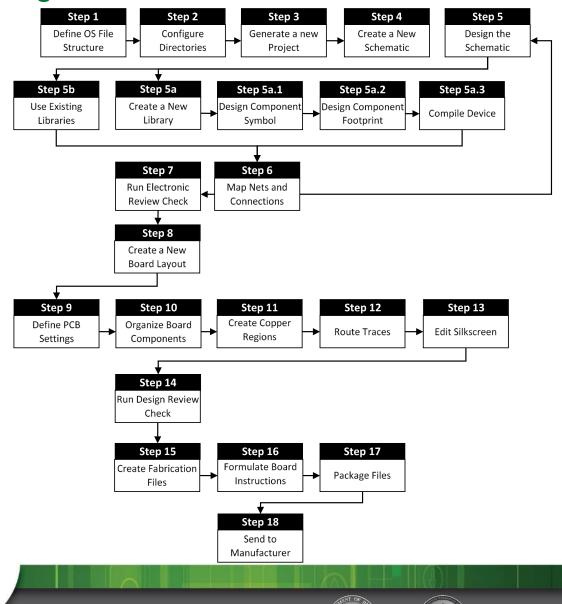






# **Two-Layer PCB Design**

- Goal is to design a microcontroller board that will control three LEDs.
- Requirements:
  - **Dimensions**: about 1.5 inches x 1.5 inches x 0.0625 inches (length x width x height)
  - Lead Free: yes
  - Material: FR4
  - Board Color: green
  - Copper Weight: 1 oz
  - Silkscreen Color: white
  - Silkscreen Placement: top layer only (although design may have text on bottom layer)
  - Plated Through Holes: yes



## **Two-Layer PCB Design - Step 1: OS File Structure**

🔵 🔾 🔻 📗 C:\Users\kkwashnak\[	Desktop\Kwashnak	•	Search Kw
Organize 👻 Include in library 👻	Share with 🔻	New folder	:= - 1 🔞
🔆 Favorites	Name	Date modified	Туре
	퉬 EAGLE 5.3.0 CD	8/18/2020 3:59 PM	File folder
📃 Desktop	퉬 Eagle Libraries	8/20/2020 8:17 PM	File folder
🥽 Libraries	퉬 Projects	8/19/2020 1:53 PM	File folder
🥦 kkwashnak			
👰 Computer			
📬 Network			
📴 Control Panel			
👿 Recycle Bin			
퉬 Kwashnak			
퉬 VAULT			
	•	III	
3 items			

Create folders that will house project:

- Library
- Project
  - Schematic
  - Board
  - References
  - Design Rules

DoDIAC

- Fab
- Notes



#### **Two-Layer PCB Design - Step 2: Configure Directories**

🖊 Control Pa	inel - (	C:\Use	ers\kkwa	shnak\Deskto	p\Kwashnak\Proj	jects\Exam	ample - EAGLE 5.3.0 Pr 👝 🗉 💌				
File View	Opti	ions	Window	v Help							
Vame		Direct	tories		Description						
	uage I	Wind Progra	interface ow posit		Libraries Design Rules User Language F Script Files CAM Processor Examples Folder	Jobs	15				
			ſ	📕 Directo	ories						
				Libraries		\$EAGLED	EDIR \br;C: \Users \kwashnak \Desktop \Kwashnak \Eagle Libraries				
				Design Ru	lles	\$EAGLEDIR\dru					
				User Lang	juage Programs	\$EAGLED	\$EAGLEDIR \ulp				
				Scripts		\$EAGLED	EDIR \\$cr				
				CAM Jobs		\$EAGLED	\$EAGLEDIR \cam				
				Projects		\$HOME\e	E\eagle;\$EAGLEDIR\projects\examples;C:\Users\kkwashnak\Desktop\Kwashnak\Projects				
							OK Cancel Browse				

- Add location paths to EAGLE's directories
- Adding directories requires a ';' directly after the previous path; do not add a space before the next location



#### **Two-Layer PCB Design - Step 3: Generate a New Project**

🖊 Control Pa	anel - C:\Users\kkw	ashnak\Desktop\Kwashnak\Pro	ojects\Example - EAGLE 5.3.0 Pr 💼 🔳 💌
File View	Options Windo	w Help	
Name	Directories	. Description	
<ul> <li>Scripts</li> <li>CAM Jobs</li> <li>Projects</li> <li>         i ex     </li> </ul>	User interfac Window pos uage Programs	Libraries	Jobs
		<b>#</b> Directories	
		Libraries	\$EAGLEDIR\br;C:\Users\kkwashnak\Desktop\Kwashnak\Eagle Libraries
		Design Rules	\$EAGLEDIR\dru
		User Language Programs	\$EAGLEDIR \ulp
		Scripts	\$EAGLEDIR\scr
		CAM Jobs	\$EAGLEDIR\cam
		Projects	\$HOME\eagle; \$EAGLEDIR \projects \examples; C: \Users \kkwashnak \Pesktop \Kwashnak \Projects
			OK Cancel Browse

Create folders that will house project

– Library

- Project
  - Schematic
  - Board
  - References
  - Design Rules

DoDIAC

- Fab
- Notes

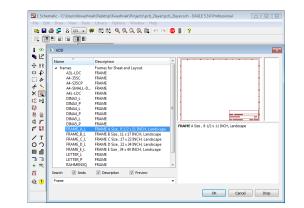


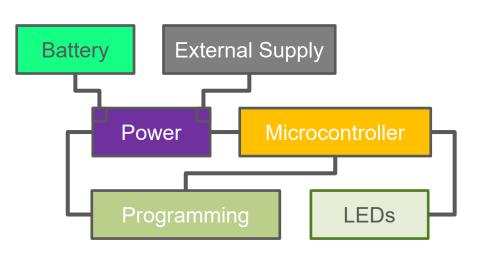
## **Two-Layer PCB Design - Step 4: Create a New Schematic**

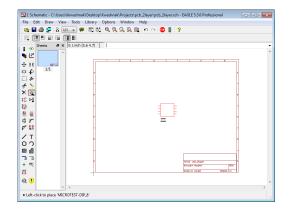
- Research
   components
- Create a new schematic
- Formulate a systems diagram
- Activate/create
   libraries
- Diagram circuit
- Create Bill of Materials (BOM)

File View Options Window Help					
Name	Description		Empty Project		
<ul> <li>Litarries</li> <li>Design Rules</li> <li>User Language Programs</li> <li>Scripts</li> <li>CAM Jobs</li> <li>Projects</li> <li>aggle</li> <li>aga Projects</li> <li>aga Projects</li> </ul>	Design Rules User Language Pr Script Files CAM Processor Jo Examples Folder	-	Use the context mi schematic or board	nu to create new files within this project	
4 🦉 pcb_2layer	Empty Project	Clos	e Project		
<ul> <li>methods</li> <li>methods</li></ul>	Empty Project	Clos	-	Schematic	
▲ 🚎 pcb_2layer	Empty Project		∕ → ame	Schematic Board Library	
🔺 🚈 pcb_2layer	Empty Project	New Rena Cop Dele	ame y te	Board	
▲ 📴 pcb_2layer	Empty Project	New Rena Cop Dele	ame y	Board Library	

ile View Options	Window Help			
Vame		Description	*	
▲ Libraries			=	
🔺 🤤 lbr	Use all	Libraries		
elektro	Use none	Libraries for Electric		
		19-Inch Slot Euroca		
⊳ 📕 40xx.lbr		CMOS Logic Device		
		41xx Series Devices		
45xx.lbr		CMOS Logic Device		
Ac-log	ic.lbr	TTL Logic Devices,		
⊳ 🟉 74ttl-din	lbr	TTL Devices with DL		
⊳ 📕 74xx-eu.I	br	TTL Devices, 74xx S		
Axx-little     Axx-little	e-de.lbr	Single and Dual Gat		
Axx-little     Axx-little	e-us.lbr	Single and Dual Gat		
⊳ 📕 74xx-us.I	br	TTL Devices, 74xx S		
b // 251xx.lbr		75xxx Series Devices		
D // // // // // // // // // // // // //	echnologies.lbr	Agilent Technologies		
	er 🛛	Allegro MicroSyste		
	clone-II.lbr	ALTERA Cyclone II F		
	clone-III.lbr	ALTERA Cyclone III		
		Altera Programmab		
⊳ 🟉 am29-m	emory.lbr	Advanced Micro De	-	





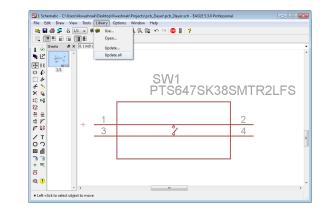


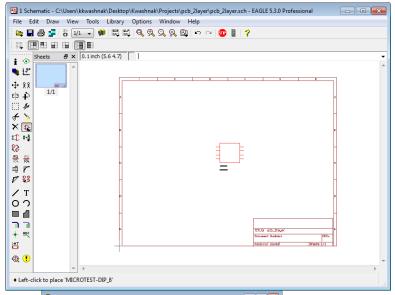


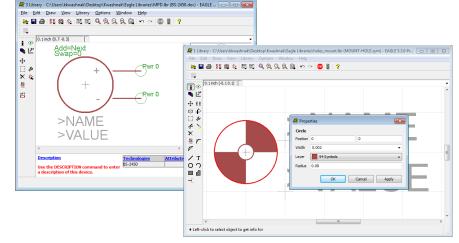
#### **Two-Layer PCB Design - Step 5: Design the Schematic**

- Populate schematic with components
- Roughly place and organize hardware
- Use existing libraries
- Import libraries
- Modify existing devices (variants)
- Create new library
  - Device
    - Symbol
    - Package/footprint

File View Options Window Help					
lame ^	Description	-	Libraries		
Libraries		E	The component libraries supplied with		
🔺 🔄 lbr	Libraries		EAGLE have been compiled with great care		
elektro	Libraries for Electric		as an additional service to you, our		
I9inch.lbr	<ul> <li>19-Inch Slot Euroca</li> </ul>		customer. However, the large number of available components and suppliers of		
⊳ 🧾 40xx.lbr	<ul> <li>CMOS Logic Device</li> </ul>		available components and suppliers of these components means that the		
41xx.lbr	<ul> <li>41xx Series Devices</li> </ul>		occasional discrepancy is unavoidable.		
45xx.lbr	<ul> <li>CMOS Logic Device</li> </ul>		Please note, therefore, that CadSoft takes		
74ac-logic.lbr	<ul> <li>TTL Logic Devices,</li> </ul>		no responsibility for the complete accuracy		
74ttl-din.lbr	<ul> <li>TTL Devices with DI</li> </ul>		of information included in library files.		
74xx-eu.lbr	<ul> <li>TTL Devices, 74xx S.</li> </ul>		Additional new libraries, that have not yet		
74xx-little-de.lbr	<ul> <li>Single and Dual Gat</li> </ul>		been officially released, can be found on		
A 74xx-little-us.lbr	<ul> <li>Single and Dual Gat</li> </ul>		CadSoft's internet site at the download		
74xx-us.lbr	<ul> <li>TTL Devices, 74xx S.</li> </ul>		section of		
Figure 10 August 10 Aug	<ul> <li>75xxx Series Devices</li> </ul>		http://www.cadsoftusa.com.		
agilent-technologies.lbr	<ul> <li>Agilent Technologie</li> </ul>	s	Use the ADD command in the Schematic		
allegro.lbr	<ul> <li>Allegro MicroSyste.</li> </ul>		Editor or Layout Editor window to search		
altera-cyclone-II.lbr	<ul> <li>ALTERA Cyclone II F</li> </ul>		for a certain device or package!		
altera-cyclone-III.lbr	ALTERA Cyclone III		Information about defining your own		
Altera.lbr	<ul> <li>Altera Programmab</li> </ul>		libraries can be found in the file library.txt		
am29-memory.lbr	<ul> <li>Advanced Micro De</li> </ul>		in the doc directory.		



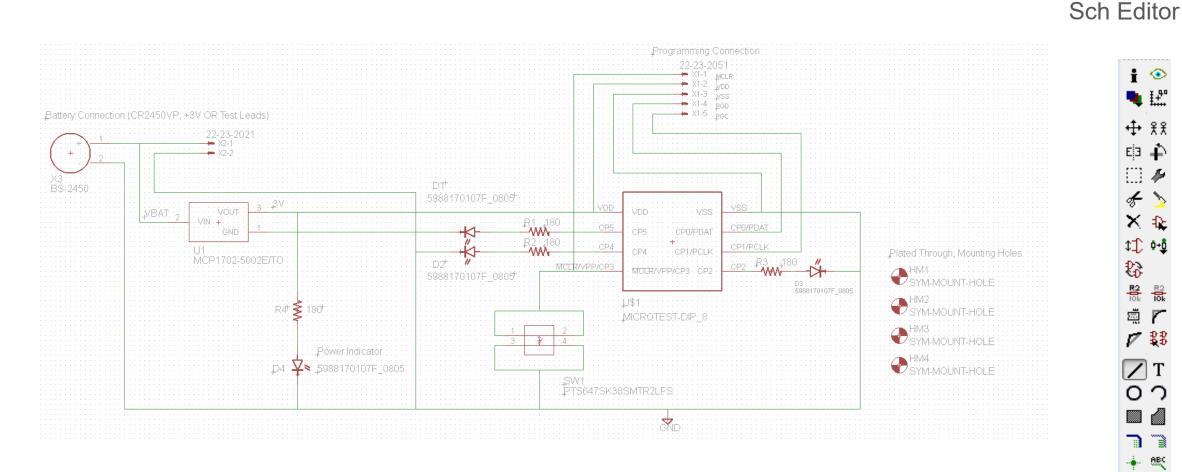








## **Two-Layer PCB Design - Step 6: Map Nets and Connections**



- Organize components •
- Name nets •

- Add labels to describe system
- Add nonlinked devices •





÷

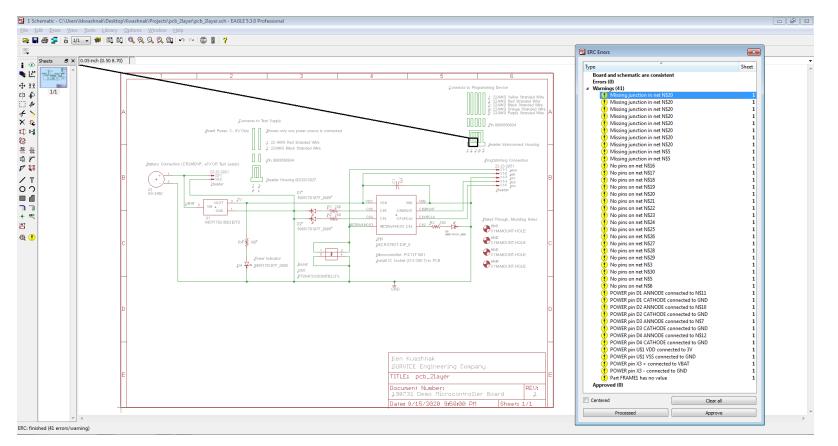
14

N

R2 IOk

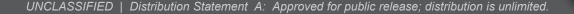
ABC

#### **Two-Layer PCB Design - Step 7: Run Electronic Review Check**

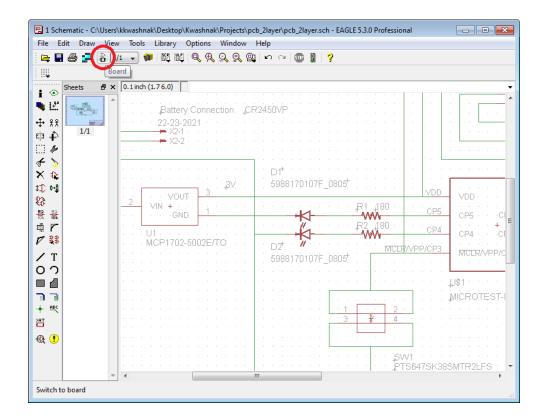


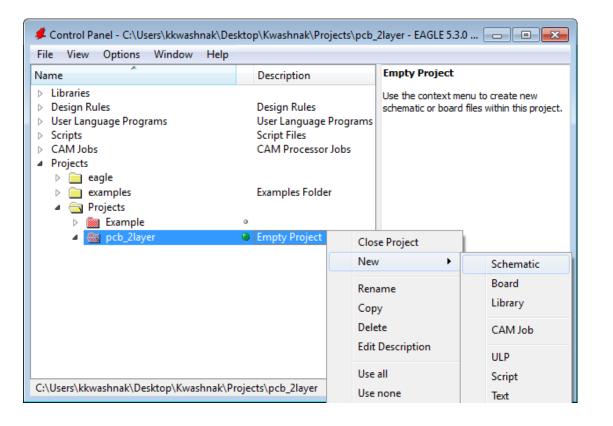
- Check schematic for errors:
  - Pin-type assignments
  - Missing connections
  - Unintended grounding of nets
  - Connection diagramming

A



#### **Two-Layer PCB Design - Step 8: Create a New Board Layout**

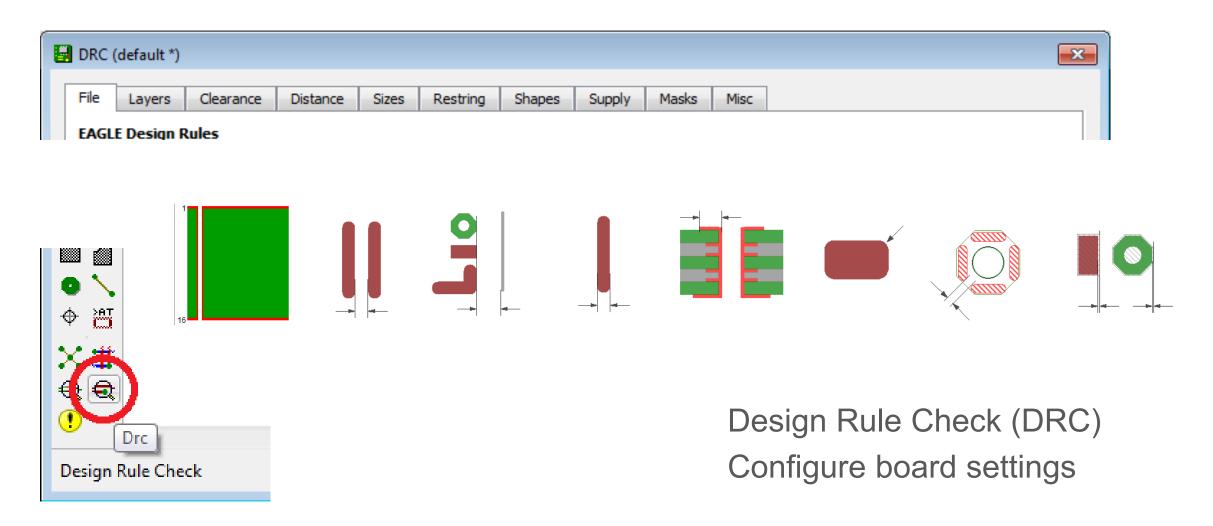




A



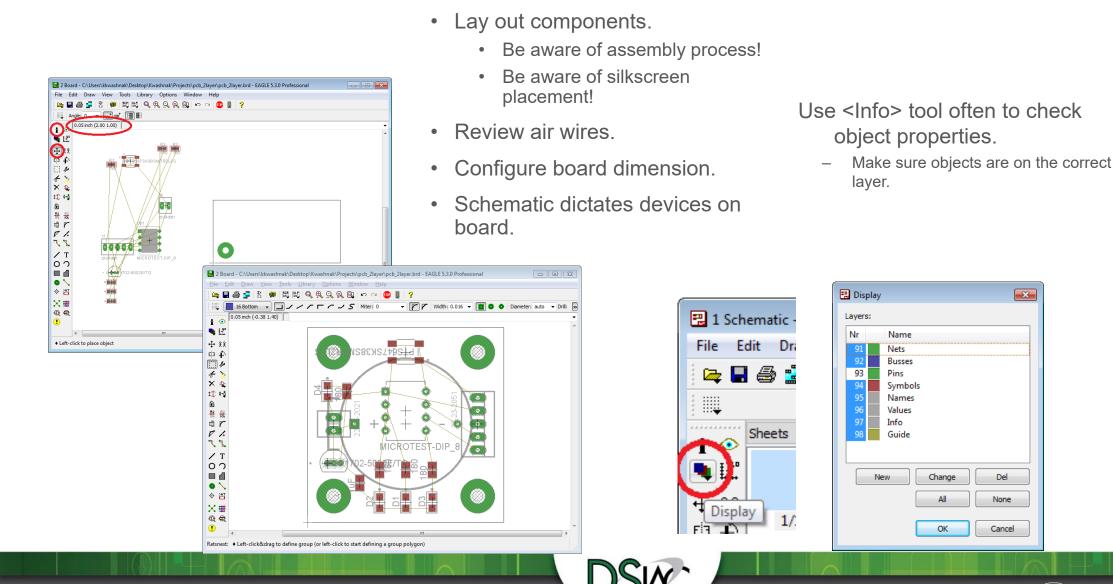
## **Two-Layer PCB Design - Step 9: Define PCB Settings**





DODIAC

## **Two-Layer PCB Design - Step 10: Organize Components**



#### **Brd Editor**

۰

Į.#"

4

÷ 1,8

ΕЗ

F

X 🕹

ឌុី 🏹

ቀ 👸

×≇

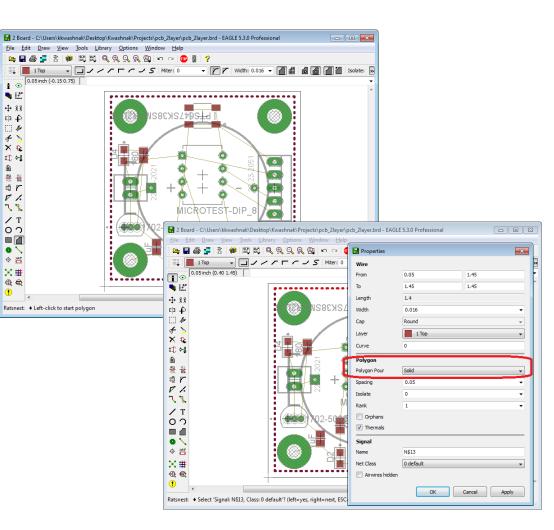
**Q Q** 

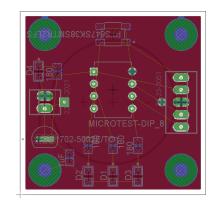
۲

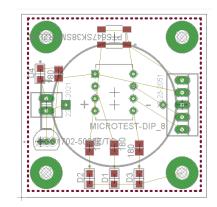
\$‡ ••₫

### **Two-Layer PCB Design - Step 11: Create Copper Regions**

- Create an area on the board where copper will be poured.
- Configure region settings.
- Regions will be on top and bottom of the board.

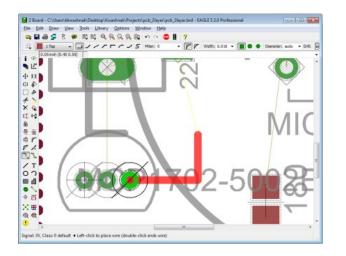


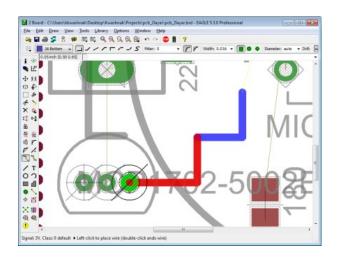


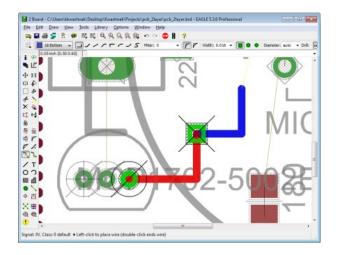




## **Two-Layer PCB Design - Step 12: Route Traces**

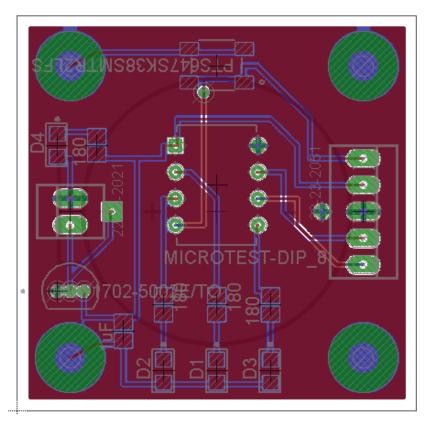






- Use air wires as a reference
- When routing, change layers with layer dropdown to go from top to bottom of the board (creates a Via)
- When routing, right-click cycles through wire type
- Auto-router







## Two-Layer PCB Design - Step 12: Route Traces (cont.)

	•••••	
🛃 Autorouter Setup		
General Busses Route Optimize1	Optimize2	Optimize3 Optimize4
Preferred Directions	Routing Grid	50 mil
1 Top / 🔻 9 Route9 N/A 🔻	Via Shape	Round
2 Route2 N/A 🔻 10 Route10 N/A 👻		
3 Route3 N/A 🔻 11 Route11 N/A 👻		
4 Route4 N/A 🕶 12 Route12 N/A 💌		
5 Route5 N/A 🕶 13 Route13 N/A 💌		
6 Route6 N/A 🕶 14 Route14 N/A 💌		
7 Route7 N/A 🕶 15 Route15 N/A 💌		
8 Route8 N/A 🕶 16 Bottom / 💌		Load Save as
		OK Select Cancel

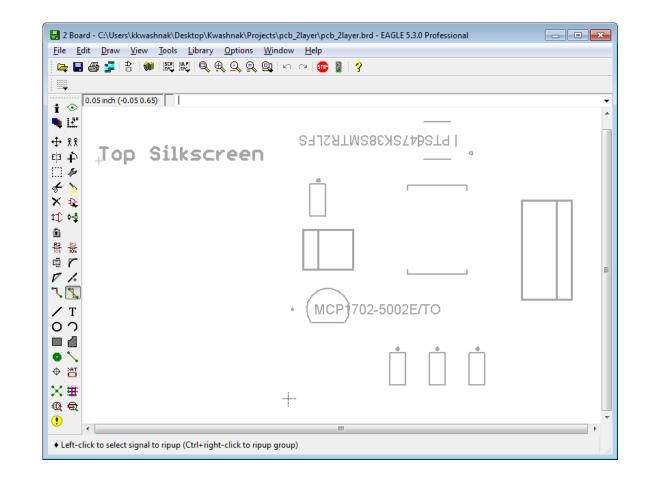
Symbol	Preferred Direction
-	Left to Right
	Up and Down
/	45 deg, Bottom Left to Top Right
\	45 deg, Top Left to Bottom Right
*	No Preference
Auto	EAGLE will access and optimize

CAD



## Two-Layer PCB Design - Step 13: Edit Silkscreen

- 21 tPlace,
- 22 bPlace
- 25 tNames
- 26 bNames
- <Text> tool
  - Either layer
    '21 tPlace' or
    '22 bPlace'
- Helpful to turn on/off layers





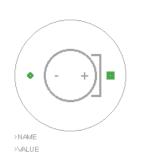


#### **Two-Layer PCB Design - Step 14: Run Design Review Check**

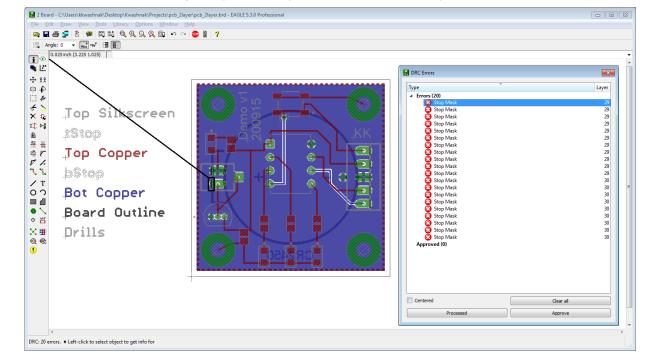
DRC (default *)					
			A L Mine		
File Layers Clearand	e Distance Sizes Restri	ng Shapes Suppl	y Masks Misc		
Check grid					
Check angle					
Check font					
Check restrict					
	all pads, smds, vias and wires in sig				
			Check	Select	Cancel Apply
3 Library - C:\Users\kkwashnak\Desktop\Kwashna e Edit Draw Vjew Library Options W	k\Eagle Libraries\MPD.lbr (BS-2450.dev) - EAGLE				
= E @ 38 @ 0. KK K Q Q Q					
Add=Next	*			>	
Add=Next Swap=0	(·O)				
					$\langle \rangle$

 Die Lota (und vollage)
 Letter (und vollage)

 Die State (und vollage)
 Letter (und vo



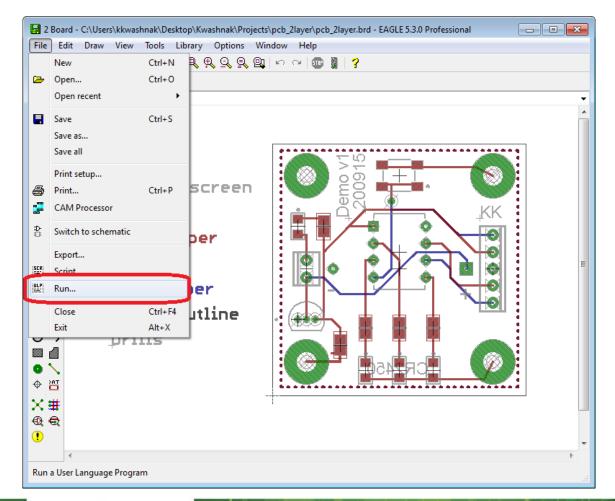
- DRC might find numerous warnings or errors
  - Silkscreen symbols might interfere with pin holes.
    - Change board requirements
    - Change symbol (create a variant)







- ULPs
  - drillcfg.ulp
    - Configures drill holes
- CAM Processor
  - excellon.cam
    - Generates drill data
  - gerb274x.cam
    - Layers information







- ULPs
  - drillcfg.ulp
    - Configures drill holes
- CAM Processor
  - excellon.cam
    - Generates drill data
  - gerb274x.cam
    - Layers information

Eagle: Drill Configuration	<b>—</b>
Select unit for output file mm inch	OK Quit
Edit only if you are sure what you	
T01 0.018in T02 0.031in T03 0.039in T04 0.125in	
Ok	
Cancel	



output = .drl

- ULPs
  - drillcfg.ulp
    - Configures drill holes
- CAM Processor
  - excellon.cam
    - Generates drill data
  - gerb274x.cam
    - Layers information

Job	Style	Nr	Layer	*
Section Generate drill data Prompt Output Device EXCELLON  File /Projects/pcb_2layer/Fab/%N.drd Offset X Oinch Y Oinch	<ul> <li>Mirror</li> <li>Rotate</li> <li>Upside down</li> <li>pos. Coord</li> <li>Quickplot</li> <li>Optimize</li> <li>Fill pads</li> </ul>	34 35 36 37 38 39 40 41 42 43 44 45 46 47 48 49 51	tFinish bFinish tGlue bGlue tTest bTest tKeepout tRestrict bRestrict vRestrict Drills Holes Milling Measures Document Reference tDocu bDocu	H H

# output = drd and .dri



- ULPs
  - drillcfg.ulp
    - Configures drill holes
- CAM Processor
  - excellon.cam
    - Generates drill data
  - gerb274x.cam
    - Layers information

Top Silkscreen	Top Stop	Top Copper	Bottom Copper	Bottom Stop	Bottom S	ilkscreen	Board Outline	Drills and Hole
Job Section Top S Prompt Output Device File Offset X Oinch Y Oinch	Silkscreen	2S274X		Style Mirror Rotate Upside down Ø pos. Coord Quickplot Ø Optimize Ø Fill pads	Nr	Layer 13 Route 14 Route 15 Route 15 Route 16 Botto 17 Pads 18 Vias 19 Unrol 20 Dime 21 tPlac 23 tOrig 24 bOrig 25 tNarr 26 bNar 27 tValue 28 bValu 29 tStop 30 bStop 31 tCrea	e13 e14 e15 om uted insion e ins jins ies ies es ies	
			Deep	ess Job Proces	s Section	Descript	ion Add	Del

# output = .tslk





- ULPs
  - drillcfg.ulp
    - Configures drill holes
- CAM Processor
  - excellon.cam
    - Generates drill data
  - gerb274x.cam
    - Layers information

op Silkscreen	Top Stop	Top Copper	Bottom Copper	Bottom Stop	Bottom Silkso	reen Board	d Outline	Drills and Hole
Job Section Top S Prompt Output Device File Offset X Oinch Y Oinch	GERBER_F	15274X		Style Mirror Rotate Upside down Ø pos. Coord Quickplot Ø Optimize Ø Fill pads	20 21 22 23 24 25 26 27 28 29 30 31 32 33 34 35 36	Layer Unrouted Dimension tPlace bPlace tOrigins tNames bNames tValues bValues tStop tCream bCream tFinish bFinish tGlue bGlue tTest		
			Proc	ess Job Proces	s Section D	escription	Add	Del

## output = .tstp



- ULPs
  - drillcfg.ulp
    - Configures drill holes
- CAM Processor
  - excellon.cam
    - Generates drill data
  - gerb274x.cam
    - Layers information

Top Silkscreen	Top Stop	Top Copper	Bottom Copper	Bottom Stop	Bottom Silkso	ottom Silkscreen Board		Drills and Hole
Job Section Top ( Prompt Output Device File Offset X Oinch Y Oinch	Copper GERBER_F	2S274X		Style Mirror Rotate Upside down Ø pos. Coord Quickplot Ø Optimize	2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18	Layer Top Route2 Route3 Route4 Route5 Route6 Route7 Route8 Route9 Route1 Route1 Route1 Route1 Route1 Route1 Route1 Route1 Route3 Route3 Route4 Route5 Route4 Route5 Route6 Route5 Route6	0 1 2 3 4 5	E
			Proc	ess Job Proces		Unrout		Del

# output = .tcpr



- ULPs
  - drillcfg.ulp
    - Configures drill holes
- CAM Processor
  - excellon.cam
    - Generates drill data
  - gerb274x.cam
    - Layers information

Top Silkscreen	Top Stop	Top Copper	Bottom Copper	Bottom Stop	Bottom Silkscreen		Board Outline	Drills and Hole
Job Section Botte Prompt Output Device File Offset X Oinch Y Oinch	GERBER_F	LS274X		Style Mirror Rotate Upside down Style S	10 11 12 13 14 15 16 17 18 19 20 21 22 23 24	Layer Route9 Route10 Route11 Route13 Route13 Route13 Route13 Route13 Bottom Pads Vias Unrouted Dimensio tPlace tOrigins bOrigins tNames	on	
						bNames tValues		-

## output = .bcpr



- ULPs
  - drillcfg.ulp
    - Configures drill holes
- CAM Processor
  - excellon.cam
    - Generates drill data
  - gerb274x.cam
    - Layers information

·
E
-

# output = .bstp



- ULPs
  - drillcfg.ulp
    - Configures drill holes
- CAM Processor
  - excellon.cam
    - Generates drill data
  - gerb274x.cam
    - Layers information

Nr     Layer       13     Route13       14     Route14       15     Route15       16     Bottom       17     Pads       18     Vias       19     Unrouted       20     Dimension       21     tPlace       22     bPlace
23 tOrigins 24 bOrigins 25 tNames 26 bNames 27 tValues 28 bValues 29 tStop 30 bStop 31 tCream

# output = .bslk





- ULPs
  - drillcfg.ulp
    - Configures drill holes
- CAM Processor
  - excellon.cam
    - Generates drill data
  - gerb274x.cam
    - Layers information

Top Silkscreen	Top Stop	Top Copper	Bottom Copper	Bottom Stop	Bottom Silks	creen Board Outline	Drills and Hole
Job Section Board Prompt Output Device File Offset X Oinch Y Oinch	GERBER_R	S274X		Style Mirror Rotate Upside down Ø pos. Coord Quickplot Ø Optimize Ø Fill pads	14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30	Layer Route13 Route14 Route15 Bottom Pads Vias Unrouted Dimension tPlace tOrigins toPlace tOrigins tNames bOrigins tNames bValues tValues tStop bStop tCream	
			Proc	ess Job Proces	s Section	Description Add	Del

# output = .dout





- ULPs
  - drillcfg.ulp
    - Configures drill holes
- CAM Processor
  - excellon.cam
    - Generates drill data
  - gerb274x.cam
    - Layers information

Top Silkscreen	Top Stop	Top Copper	Bottom Copper	Bottom Stop	Bottom Silkso	reen Board Outline	Drills and Hole
Job Section Drills Prompt Output Device File Offset X 0inch Y 0inch	and Holes	.5274X		Style Mirror Rotate Upside down Ø pos. Coord Quickplot Ø Optimize Ø Fill pads	34 35 36 37 38 39 40 41 42 43 44 45 46 47 48 49 51	Layer tFinish bFinish tGlue bGlue tTest bTest tKeepout bKeepout tRestrict bRestrict vRestrict Drills Holes Milling Measures Document Reference tDocu bDocu	
			Proc		s Section D	escription Add	Del

## output = .ddrl



- ULPs
  - drillcfg.ulp
    - Configures drill holes
- CAM Processor
  - excellon.cam
    - Generates drill data
  - gerb274x.cam
    - Layers information

p Silkscreen	Top Stop	Top Copper	Bottom Copper	Bottom Stop	Bottom	n Silkscreen	Board Outline	Drills and Holes		
lob vection Top S vrompt Dutput Device File Offset Oinch	GERBER_F	NS274X		Style Mirror Rotate Upside down Upside down Style Dyske down Sty	Nr	Laye 13 Rout 14 Rout 15 Rout 15 Rout 16 Botto 17 Pads 19 Unro 20 Dime 21 tPlac 22 bPlac 23 tOrig 25 tNan 26 bNar 27 tValu 28 tOrig 29 tStop 30 bSto	e13 e14 e15 om uted ension e e e gins hes hes hes es es es o		Generates Extended G ierber Format feight sections that generates data for a tw files that contain data for:	
ers\kkwashn	ak\Desktop\I	Kwashnak\Proj	Proc ects\pcb_2layer\p		s Section	31 tCrea	im		ts of eight sections that generates data for erber files that contain data for:  k - bopr *.bslk out	a two layer board

 $\langle br \rangle$ 



Cancel

Undo

Redo

OK

## **Two-Layer PCB Design - Step 16: Formulate Instructions**

# Contact Information

Software Used Tracing History Requirements Board Information Fabrication File Associations

Description of Graphics Files

Author	Ken Kwashnak
Author Email	***@***.***
Author Phone	• • (***)***_***
Date	September 23, 2020
Board Name	Demo Board (pcb_2layer)
Board Version	1.0 (baseline)
Board Dimension	1.5" x 1.5" x 0.063"
Board Material	FR4
Copper Weight	1 oz
Lead Free	Yes
Soldermask	Both Sides
Soldermask Color	Green
Silkscreen	Both Sides
Silkscreen Color	White
	files were processed from EAGLE v5.3.0:
- pcb_2layer.drl	(Drill List)
<ul> <li>pcb_2layer.drd</li> </ul>	(excellon.cam, Drill Location Information)
- pcb_2layer.dri	(excellon.cam, Drill Location Information)
<ul> <li>pcb_2layer.tslk</li> </ul>	(Gerber274x.cam, Top Silkscreen)
<ul> <li>pcb_2layer.tstp</li> </ul>	(Gerber274x.cam, Top Stop)
<ul> <li>pcb_2layer.tcpr</li> </ul>	(Gerber274x.cam, Top Copper)
<ul> <li>pcb_2layer.bcpr</li> </ul>	(Gerber274x.cam, Bottom Copper)
<ul> <li>pcb_2layer.bstp</li> </ul>	(Gerber274x.cam, Bottom Stop)
<ul> <li>pcb_2layer.bslk</li> </ul>	(Gerber274x.cam, Bottom Silkscreen)
<ul> <li>pcb_2layer.dout</li> </ul>	(Gerber274x.cam, Board Outline)
<ul> <li>pcb_2layer.ddrl</li> </ul>	(Gerber274x.cam, Drills and Holes)
- pcb_2layer.gpi	(Gerber274x.cam, Photoplotter)

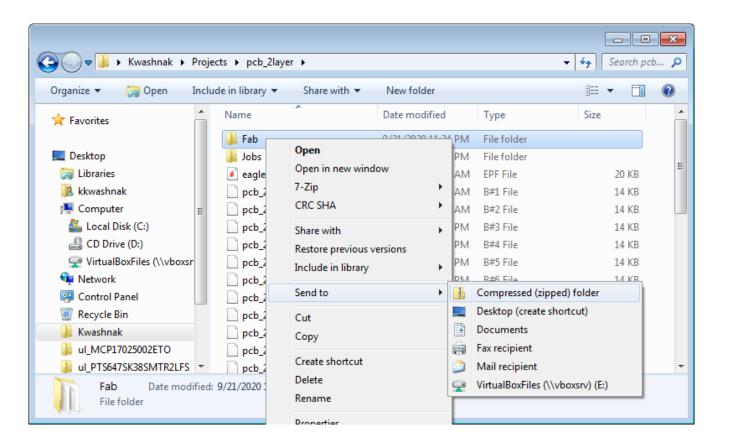
Additional Notes:

- Plated Through Holes, Sized for No 4 Holes, Quantity 4



## **Two-Layer PCB Design - Step 17: Package Files**

- Compress to a single folder
- Rename with tracing/ version control methodology
- Packaging may vary, depending on the manufacturer



A



### **Two-Layer PCB Design - Step 18: Send to Manufacturer**

- Read manufacturer license agreements before sending files
- Quote Auto-Gens may be fast but might not interpret your files correctly
- Call and talk to a rep in person to iron out details if you have questions or need clarifications



As of September 23, 2020, we are still operating normally.

Featured services





## Agenda

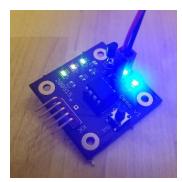
Introduction

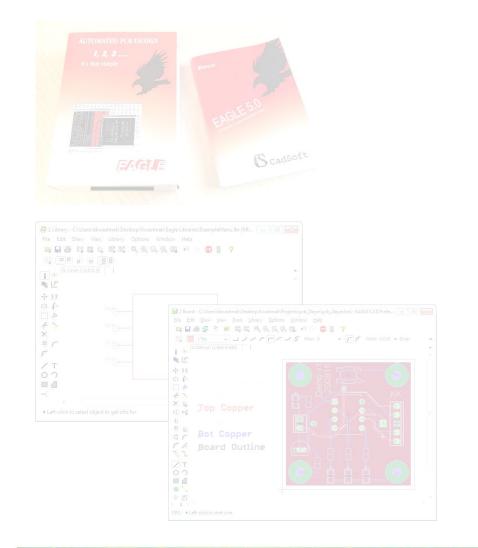
• Setup

- Creating a Component (Device)

Two-Layer PCB Design

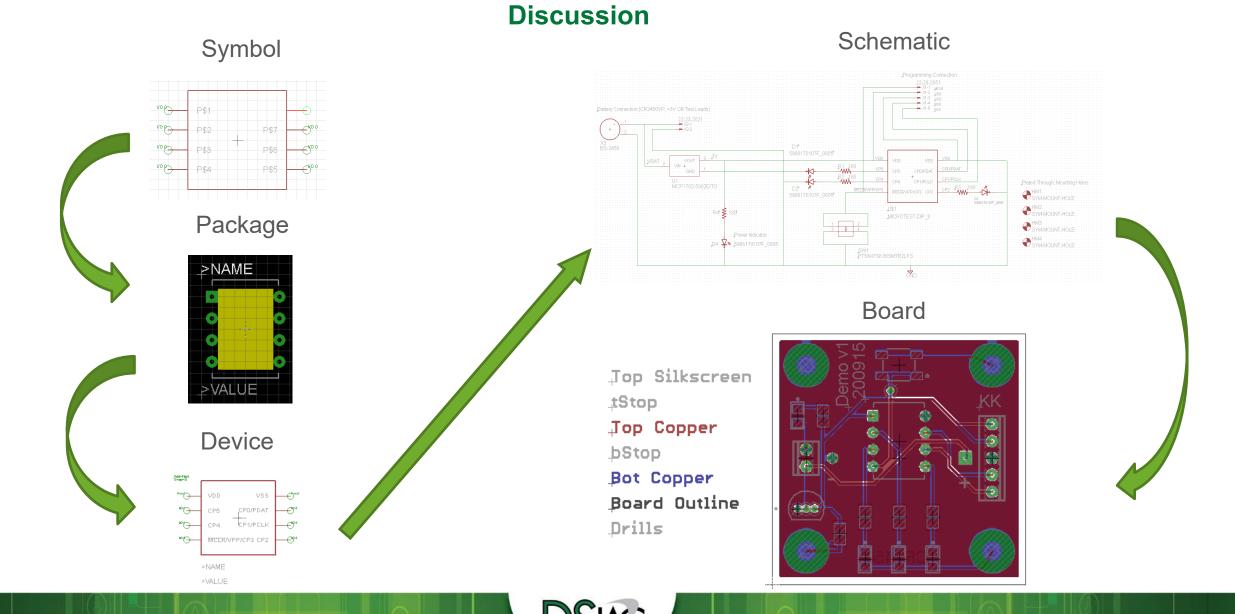
• Discussion





DODIAC

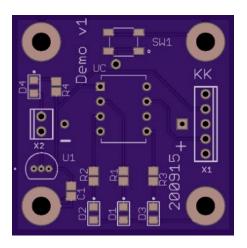
UNCLASSIFIED | Distribution Statement A: Approved for public release; distribution is unlimited.



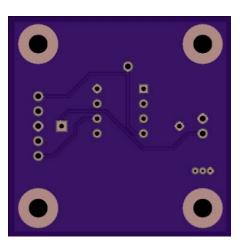
UNCLASSIFIED | Distribution Statement A: Approved for public release; distribution is unlimited.

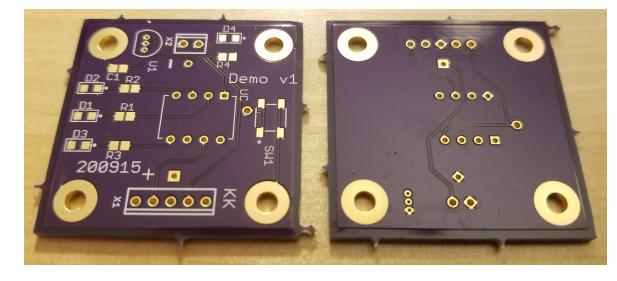


## **Discussion**



- Oshpark fabricated board
- Drag and dropped my project into quoting system (did not create CAM or Gerber files)
- About a week turnaround time
- Fairly inexpensive
- Limited onboard styles
- No live reconfiguration tools



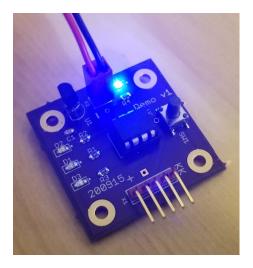






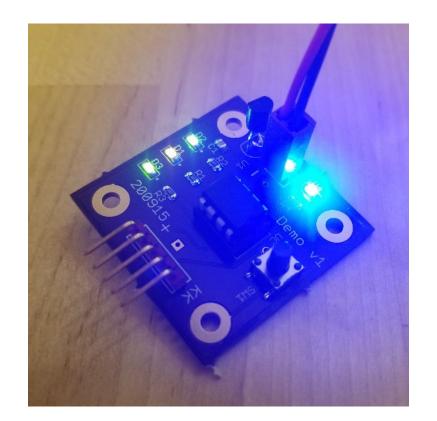
## **Discussion**

- Utilized readily available components to populate board
- Tested power checked voltages and connections
- Used MPLAB X, XC8 compiler to program microcontroller
- Tested LED functionality





• Board functions as designed, with substitute parts!







## **Appendix A - Microcontroller Code**

- 1. /\* Author: Ken Kwashnak
- 2. Contact (e): \*\*\*@\*\*\*.\*\*\*
- 3. Contact (p): (\*\*\*)\*\*\*-\*\*\*\*
- 4. Date: October 8, 2020
- 5. Platform: Program intended for PIC12(L)F1501 for testing Demo v1.0 PCB functionality.
- 6. Function: Upon power on, individual LEDs illuminate. If switch is pressed, LEDs turn off.
- 7. \*/
- 8. // define crystal frequency
- 9. #define \_XTAL\_FREQ 16000000
- 10. #include <xc.h>
- 11. // Device Configuration, pg 38-39 of Microchip DS40001615C
- 12. // In order for the device to function properly, all registers must be configured.
- 13. // Clock settings
- 14. #pragma config CLKOUTEN = 1
- 15. // Brown-Out Reset
- 16. #pragma config BOREN = 00
- 17. // Code Protection
- 18. #pragma config CP = 1
- 19. // MCLR Pin Function
- 20. // since LVP is enabled, 1, this bit is ignored
- 21. #pragma config MCLRE = 0
- 22. // Power-Up Timer
- 23. #pragma config PWRTE = 1
- 24. // Watchdog timer
- 25. #pragma config WDTE = 00

- 26. // Oscillator settings
- 27. // using internal oscillator INTOSC
- 28. #pragma config FOSC = 00
- 29. // Low Voltage Programming
- 30. // based off of the voltage supplied to uC
- 31. #pragma config LVP = 1
- 32. // Low-Power Brown-out Reset
- 33. #pragma config LPBOR = 1
- 34. // Brown-out Reset Voltage
- 35. #pragma config BORV = 1
- 36. // Stack Over/Underflow Reset
- 37. #pragma config STVREN = 0
- 38. // Flash Memory Self-Write
- 39. #pragma config WRT = 11
- 40. void init(){
- 41. // I/O, PORTA Settings
- 42. // No alternate pin functions
- 43. // RA2, RA4, RA5 = Output = LEDs
- 44. // RA3 = Input = Push Button
- 45. // Direction Control, 1 input, 0 output
- 46. TRISA = 0x0B; // Binary: 0000 1011
- 47. // No Latch Register Definitions
- 48. // Analog Select Register
- 49. // Digital only
- 50. ANSELA = 0;



#### **Appendix A - Microcontroller Code (cont.)**

51.	// Weak Pull-Up	75.
52.	// grounds input push button with switch closure, prevents floating	76.
53.	// input will read a high state, until button pressed	77.
54.	// no debouncing method or circuity, not necessary	78.
55.	// Clearing register for individual pull-up use	79.
56.	OPTION_REGbits.nWPUEN = 0;	80.
57.	// R3 Pull-up	81.
58.	WPUA = 0x08; // Binary: 0000 1000	82.
59.	}	83.
60.	void main(void){	84.
61.	// Frequency Configuration	85.
62.	OSCCONbits.IRCF = 0xF; // 1111 = 16MHz	86.
63.	// Internal Clock Configuration	87.
64.	OSCCONbits.SCS = 3;	
65.	// Initializes device, as per function above	
66.	init();	
67.	// Infinite Loop, Stay in State	
68.	// PORTAbits = reads state	
69.	// LATA = write state	
70.	//delay_ms( time in milliseconds ); note, not best if you have interrupt service routines, I	SRs

- 71. // the delay assists with the microcontroller performing the selected instruction
- // ensures there's enough time to execute the next statement 72.
- 73. // the loop essentially reads state of switch, if value is high, then write ON values to LEDs
- 74. // once the switch is pressed, input state goes low, and LEDs turn off



- 75. while(1){
- 76. if(PORTAbits.RA3){
- 77. LATA = 0b000100: // RA2
- 78. delay ms(100);
- 79. LATA = 0b010000; // RA4
- 80. \_delay\_ms(100);
- LATA = 0b100000; // RA5 81.

A

- 82. delay ms(100);
- 83. }else{
- LATA = 0b110100;84.
- 85.
- 86.
- 87. }



#### **Appendix B - Sample Library Device HTML Description**

Description of MICROTEST-DIP_8		<b>×</b>	
Headline:	MICROTEST-DIP_8		
	Author: Ken Kwashnak		
	Contact: ***@*** *** Date: August 20, 2020		
	This is a sample description file for a Library Device component.		
	······································		
1 Testing Paramet	ters		
Sample Text			
• A: This is an indented line item. T	This is <b>BOLD</b> text.		
•B: This is an indented line item. T			
C: This is an indented line item. 1			
<ul> <li>I his is a double indented</li> <li>Sample<sub>3</sub> Text<sup>1</sup></li> </ul>	d line item. Here is a combination of <b>BOLD and ITALICIZED</b> text.		
2 List of Compone	onts		
	Table Header		
	Item Description		
	1 Sample Description 1		
	2 Sample Description 2		
html			
<html> <body></body></html>			
<title> MICROTEST-DIP_8 </title> <center><b>Author</b>: Ken Kwashna</center>	ak		
> <b>Contact</b> : ***@***.***			
<b>Date</b> : August 20, 2020 <td>tor \</td> <td>=</td> <td></td>	tor \	=	
CD / DBite (10 / August 20, 2020 < 100)		-	
<center> <i> This is a sample desc</i></center>	ription file for a Library Device component.		
<h1> 1 Testing Parameters </h1> Sample Text			
<ul> <li>A: This is an indented line iter</li></ul>			
<ul> <li>C: This is an indented line iter</li></ul>	n. This is <i>ITALICIZED</i> text. m. This is <u>UNDERLINED</u> text.		
<ul><ul><li>This is a double indented <ul><ul><li>Sample<sub>3</sub>1</li></ul></ul></li></ul></ul>	d line item. Here is a combination of <b><i>BOLD and ITALICIZED</i></b> text. Text <sup>1</sup>	ıl>	
	· · · ·		
<hr/> <h1>2 List of Components </h1>			
	cing="0" bgcolor="#ffffff" width="200" align="center">		
<tread></tread>			
	" bgcolor=black> Table Header	_	
102			
	OK Cancel Unde	Redo	

<!DOCTYPE html> <html> <body> <title> MICROTEST-DIP\_8 </title> <center><b>Author</b>: Ken Kwashnak <br> <b>Contact</b>: \*\*\*@\*\*\*.\*\*\* <br> <b>Date</b>: August 20, 2020 </center> <center> <i> This is a sample description file for a Library Device component. </i> </center> <h1> 1 Testing Parameters </h1> Sample Text A: This is an indented line item. This is <b>BOLD</b> text. B: This is an indented line item. This is <i>ITALICIZED</i> text. C: This is an indented line item. This is <u>UNDERLINED</u> text. This is a double indented line item. Here is a combination of <b><i>BOLD and ITALICIZED</b></i> text. Sample<sub>3</sub> Text<sup>1</sup> <hr><h1>2 List of Components </h1> </hr> <thread> Table Header </thread> <center>Item</center> <center>Description</center> <center>1</center> <center>Sample Description 1</center> <center>2</center> <center>Sample Description 2</center> <!--This is a comment--> </body>



## **Bibliography**

1. Digikey. Kester Solder. Digikey. [Online] Digikey, 2020. [Cited: October 8, 2020.] https://www.digikey.com/en/products/detail/kester-solder/24-9574-7618/3660017. 2. Aoyue International Ltd. Int 936. Aoyue. [Online] Aoyue International Ltd, 2020. www.aoyue3d.com/en/pro/default.asp?id=35. 3. Digikey. Soldering Flux. Digikey. [Online] Digikey, 2020. [Cited: October 8, 2020.] https://www.digikey.com/en/products/detail/mg-chemicals/8341-10ML/2233037?s ... =N4IgTCBcDaIBwGYAsBGAtCgDAWwDYgF0BfIA. 4. SRA Shops. KORAD KD3005D. SRA Soldering Products. [Online] SRA Shops, 2013-2020. [Cited: October 8, 2020.] https://sra-solder.com/korad-kd3005d-precision-variable-adjustable-30v-5a-dc- ... linear-power-supply-digital-regulated-lab-grade. 5. Digikey. Test Leads. Digikey. [Online] Digikey, 2020. [Cited: October 8, 2020.] https://www.digikey.com/en/products/detail/b-k-precision/TL-5A/272826. 6. —. Fluke 117. Digikey. [Online] Digikey, 2020. [Cited: October 8, 2020.] https://www.digikey.com/en/products/detail/fluke-electronics/FLUKE-117/1506333. 7. —. Desolder Braid. Digikey. [Online] Digikey, 2020. [Cited: October 8, 2020.] https://www.digikey.com/en/products/detail/chemtronics/60-5-5/306973. 8. —. Assorted Wire. Digikey. [Online] Digikey, 2020. [Cited: October 8, 2020.] https://www.digikey.com/en/products/detail/sparkfun-electronics/PRT-11375/5956252. 9. —. Wire Strippers. Digikey. [Online] Digikey, 2020. [Cited: October 8, 2020.] https://www.digikey.com/en/products/detail/american-hakko-products-inc/CSP-30-1/8346234. 10. —. Tweezer Set. Digikey. [Online] Digikey, 2020. [Cited: October 8, 2020.] https://www.digikey.com/en/products/detail/american-hakko-products-inc/CSP-30-1/8346234. 11. —. Isopropyl. Digikey. [Online] Digikey, 2020. [Cited: October 8, 2020.] https://www.digikey.com/en/products/detail/mg-chemicals/824-1L/9181284. 12. —. Brush. Digikey. [Online] Digikey, 2020. [Cited: October 8, 2020.] https://www.digikey.com/en/products/detail/mg-chemicals/855-5/949490. 13. —. PICKit3. Digikey. [Online] Digikey, 2020. [Cited: October 8, 2020.] https://www.digikey.com/en/products/detail/microchip-technology/PG164130/2171224. 14. —. Programming Cable. Digikey. [Online] Digikey, 2020. [Cited: October 8, 2020.] https://www.digikey.com/en/products/detail/digilent-inc/240-035/4090162. 15. —. ESD Caliper. Digikey. [Online] Digikey, 2020. [Cited: October 8, 2020.] https://www.digikey.com/en/products/detail/wiha/41105/1706539. 16. —. PIC12LF1501-I/P. Digikey Electronics. [Online] 1995-2020. [Cited: September 23, 2020.] https://www.digikey.com/en/products/detail/microchip-technology/PIC12LF1501-I-P/3046619. 17. —. ICS-308-T. Digikey Electronics. [Online] 1995-2020. [Cited: September 23, 2020.] https://www.digikey.com/products/en?keywords=ics-308-T. 18. —. CR2450VP. Digikey Electronics. [Online] 1995-2020. [Cited: September 23, 2020.] https://www.digikey.com/products/en?keywords=cr2450vp. 19. —. BS2450. Digikey Electronics. [Online] 1995-2020. [Cited: September 23, 2020.] https://www.digikey.com/products/en?keywords=bs2450. 20. —. MCP1700-3002E/TO. Digikey Electronics. [Online] 1995-2020. [Cited: September 23, 2020.] https://www.digikey.com/products/en?keywords=mcp1700-3002E%2FTO. 21. —. 5988170107F. Digikey Electronics. [Online] 1995-2020. [Cited: September 23, 2020.] https://www.digikey.com/product-detail/en/dialight/5988170107F/350-. 22. —. PTS 647 SK38 SMTR2 LFS. *Digikey Electronics*. [Online] 1995-2020. [Cited: September 23, 2020.] https://www.digikey.com/product-detail/en/c-k/PTS-647-SK38-SMTR2. 23. —. CRCW0805240RFKEA. Digikey Electronics. [Online] 1995-2020. [Cited: September 23, 2020.] https://www.digikey.com/en/products/detail/vishay-dale/CRCW0805120RJNEA/1175176. 24. —. C0805C104M3RACTU. Digikey Electronics. [Online] 1995-2020. [Cited: September 23, 2020.] https://www.digikey.com/product-detail/en/kemet/C0805C104M3RACTU/399-. 25. —. 0022232051. Digikey Electronics. [Online] 1995-2020. [Cited: September 23, 2020.] https://www.digikey.com/products/en?keywords=22-23-2051.



## **Bibliography (cont.)**

- 26. —. 0022012057. *Digikey Electronics*. [Online] 1995-2020. [Cited: September 23, 2020.] https://www.digikey.com/products/en?keywords=0022012057.
- 27. —. 22-23-2021. Digikey Electronics. [Online] 1995-2020. [Cited: September 23, 2020.] https://www.digikey.com/products/en?keywords=22232021.
- 28. —. 0022012027. *Digikey Electronics*. [Online] 1995-2020. [Cited: September 23, 2020.] https://www.digikey.com/products/en?keywords=0022012027.
- 29. —. 00086508004. Digikey Electronics. [Online] 1995-2020. [Cited: September 23, 2020.] https://www.digikey.com/product-detail/en/molex/0008650804/WM2756CT-.
- 30. Autodesk. EAGLE. Autodesk EAGLE. [Online] 2020. [Cited: July 19, 2020.] www.autodesk.com/products/eagle.
- 31. —. How to get started with a new Autodesk EAGLE license. Autodesk EAGLE. [Online] 2016. [Cited: July 31, 2019.] https://www.autodesk.com/products/eagle/blog/how-to-get-started-with-a-new-autodesk-eagle-license/.
- 32. —. Free Download Eagle. Autodesk EAGLE. [Online] 2016. [Cited: July 31, 2019.] https://www.autodesk.com/products/eagle/free-download.
- 33. MIT. Eagle Help, Design Rules. MIT. [Online] 2005. [Cited: August 17, 2020.] www.mit.edu/xavid/arch/i386\_rhel4/help/127.htm.
- 34. Advanced Circuits. PCB Trace Width Calculator. Advanced Circuits. [Online] 2020. [Cited: September 4, 2020.] www.4pcb.com/trace-width-calculator.html.
- 35. —. Your Account. Advanced Circuits. [Online] [Cited: September 23, 2020.] https://www.my4pcb.com.
- 36. —. Filename Extension Summary. Advanced Circuits. [Online] 2020. [Cited: September 23, 2020.] https://www.my4pcb.com/net35/FreeDFMQuoteSpecs.aspx.
- 37. Oshpark. Let's get started! Oshpark. [Online] 2020. [Cited: September 23, 2020.] https://oshpark.com.
- 38. Microchip. MPLAB<sup>®</sup> X Integrated Development Environment (IDE). *Microchip.* [Online] Microchip Technology Inc, 2020. [Cited: October 8, 2020.] https://www.microchip. com/mplab/mplab-x-ide.
- 39. —. MPLAB<sup>®</sup> XC Compilers. *Microchip*. [Online] Microchip Technologies Inc., 2020. [Cited: October 8, 2020.] https://www.microchip.com/en-us/development-tools-tools-and-software/mplab-xc-compilers.
- 40. —. PIC12(L)F1501. PIC12F1501. [Online] 2011-2015. [Cited: October 8, 2020.] https://ww1.microchip.com/downloads/en/DeviceDoc/40001615C.pdf. DS40001615C.
- 41. w3schools. HTML Element Reference. w3schools.com. [Online] Refsnes Data, 2020. [Cited: August 20, 2020.] https://www.w3schools.com/TAGS/default.asp.
- 42. -. Color Mixer. HTML Color Mixer. [Online] Refsnes Data, 2020. [Cited: August 20, 2020.] https://www.w3schools.com/colors/colors\_mixer.asp?colorbottom=00FFFF&colortop=FFFFFF.
- 43. —. Color Picker. w3schools.com. [Online] Refsnes Data, 2020. [Cited: August 20, 2020.] https://www.w3schools.com/colors/colors\_picker.asp?colorhex=F0F8FF.
- 44. Advanced Circuits. Specs. Advanced Circuits. [Online] QuikWeb Developer, 2020. [Cited: October 8, 2020.] https://www.4pcb.com/pcb-prototype-2-4-layer-boards-specials.html.
- 45. Oshpark. Services. Oshpark. [Online] Oshpark, 2017. [Cited: October 8, 2020.] https://docs.oshpark.com/services/two-layer-hhdc/.



